

MODEL NAME : ZBW00
PCB NO :

Dell / Compal Confidential

Schematic Document

Intel Bay Trail M

OAK MLK UMA

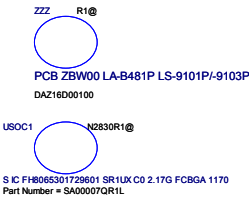
X76@ : 76 level
46@ : 46 level
3VLP@For EC +3VLP
EMC@Pop EMC Component
ESD@Pop ESD Component
XDP@XDP Component

CONN@Connector Component
@Un-pop Component
GCLK@For Green CLK function
JP@Jump Component
N3VLP@For EC +3VALW
NEMC@Un-pop EMC Component
NESD@Un-pop ESD Component
TEST@Test Point
TOUCH@For Touch Screen Function

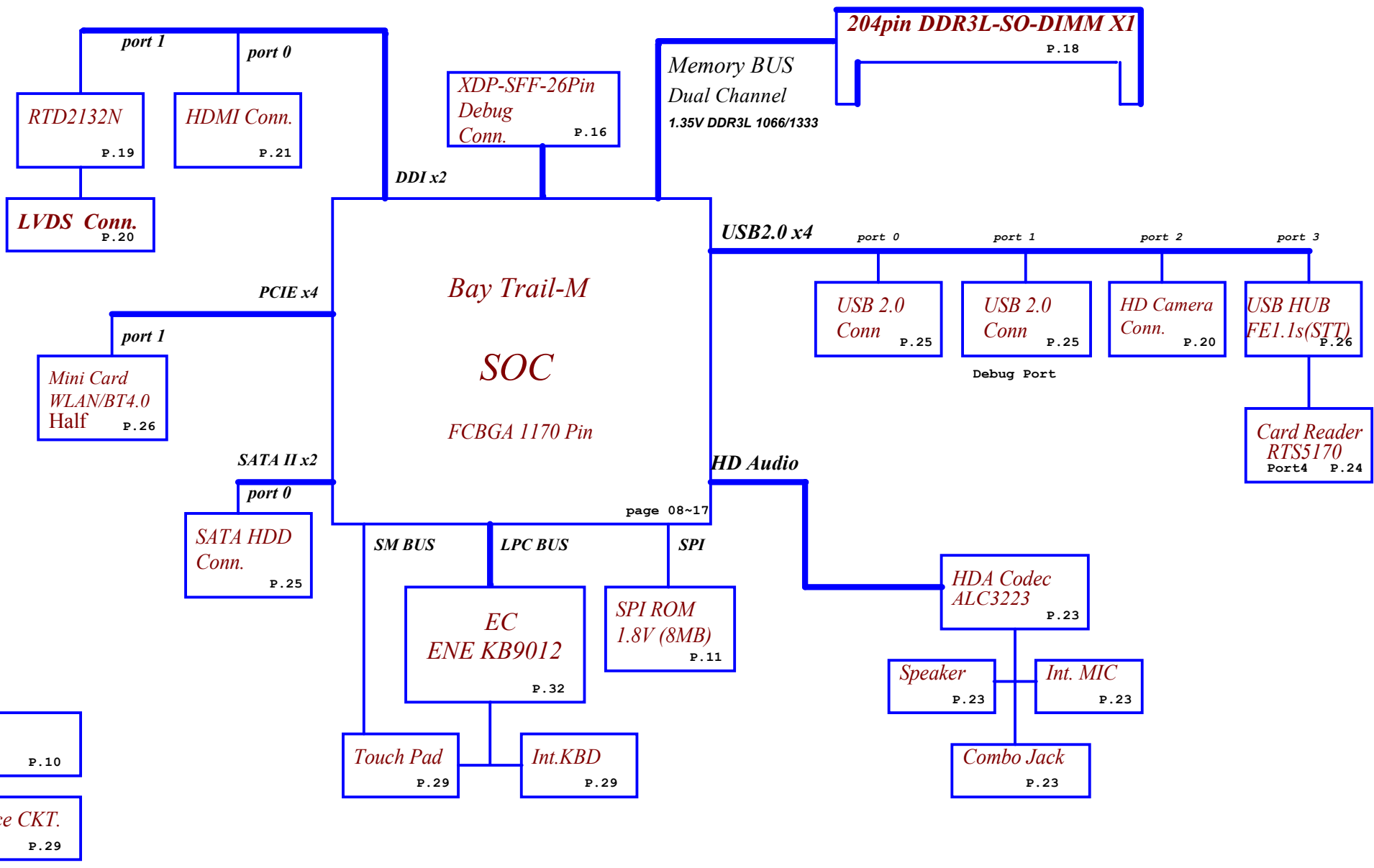
N2910@CPU Component
N3510@CPU Component
R1@PCB

2014-03-10 Rev: 2.0

BOM config
LM-43XXXXXXL01:N2910@/3VLP@/EMC@/ESD@/XDP@/3223@/JHP@
LM-43XXXXXXL01:N2910@/3VLP@/EMC@/ESD@/XDP@/3234@/JHP@



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				Date: Monday, March 10, 2014	Rev 2.0
				Sheet 1 of 42	



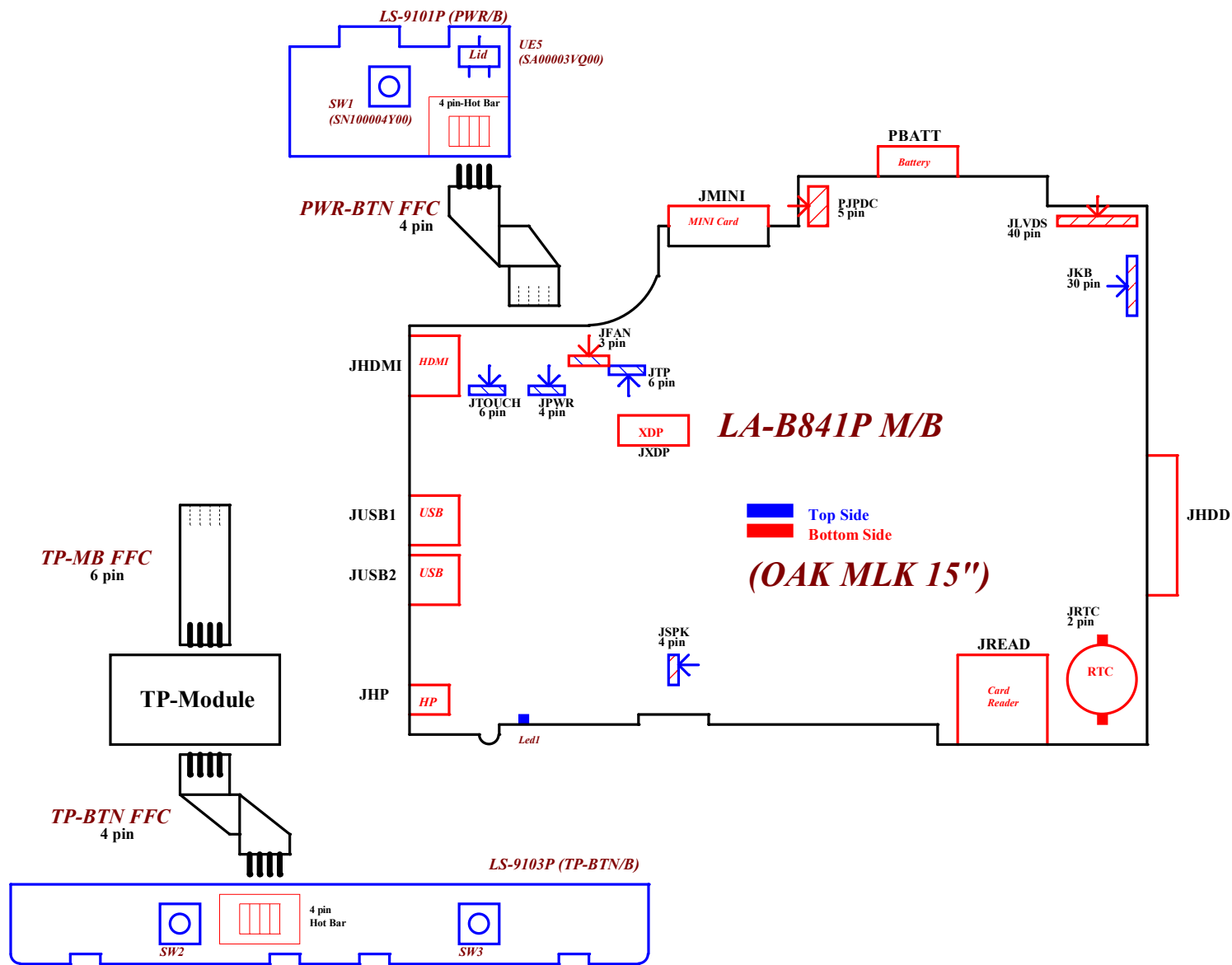
RTC CKT.
P.10

DC/DC Interface CKT.
P.29

Power Circuit DC/DC

LED/Power On/Off
P.27

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	X01
1	X02
2	X03
3	A00
4	
5	
6	
7	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
TPM	TPM@
Touch Screen	TS@
R short	RS@
Test Point	TEST@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	SoC	0x9A

SOC SM Bus address

Device	Address	Device	Address
SO-DIMM A (JDIMM1)	A0h	MINI Card	0x98
		DDR	0x82
		RTD2136	0x94

EC SM Bus2 address

43 level BOM table

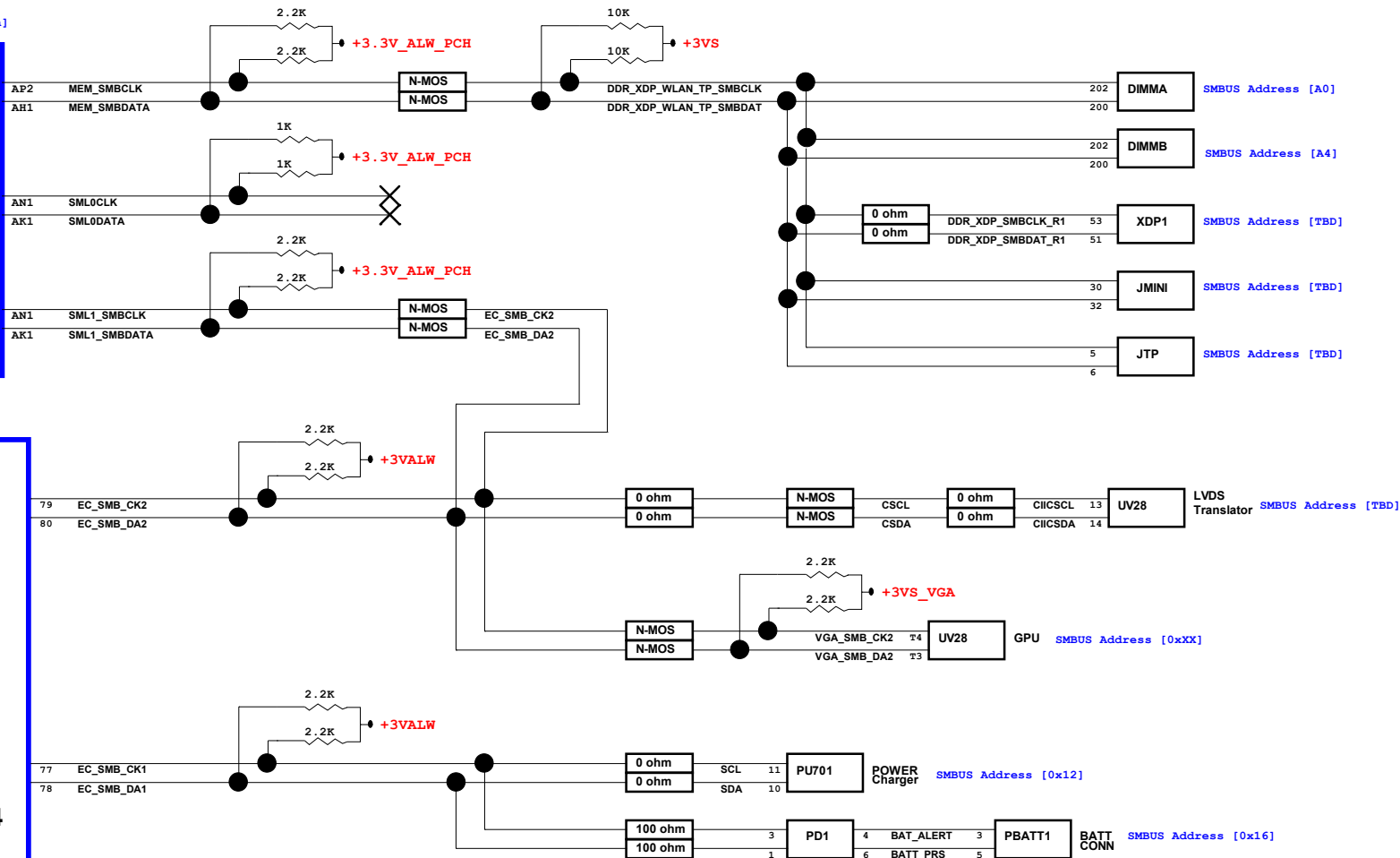
43 Level	Description	BOM Structure
4319T731L01	SMT MB AB481 ZBW00 UMA BTM HDMN2R30R1@/EMC@/ESD@/XDP@/3223@/JHP@/R1@	

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SMBUS Address [0x9a]

MCH
Shark bay

KBC
KB9012A4

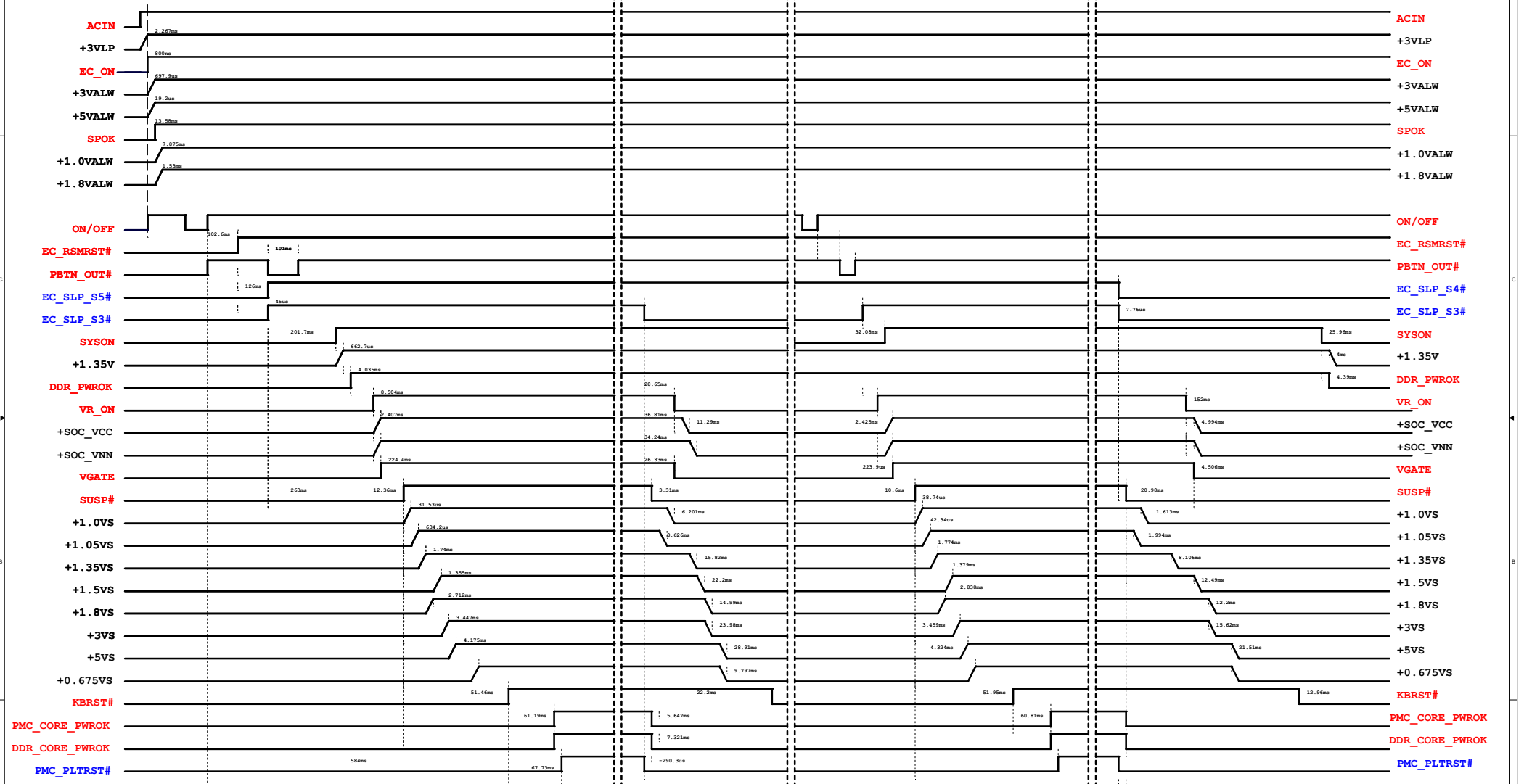


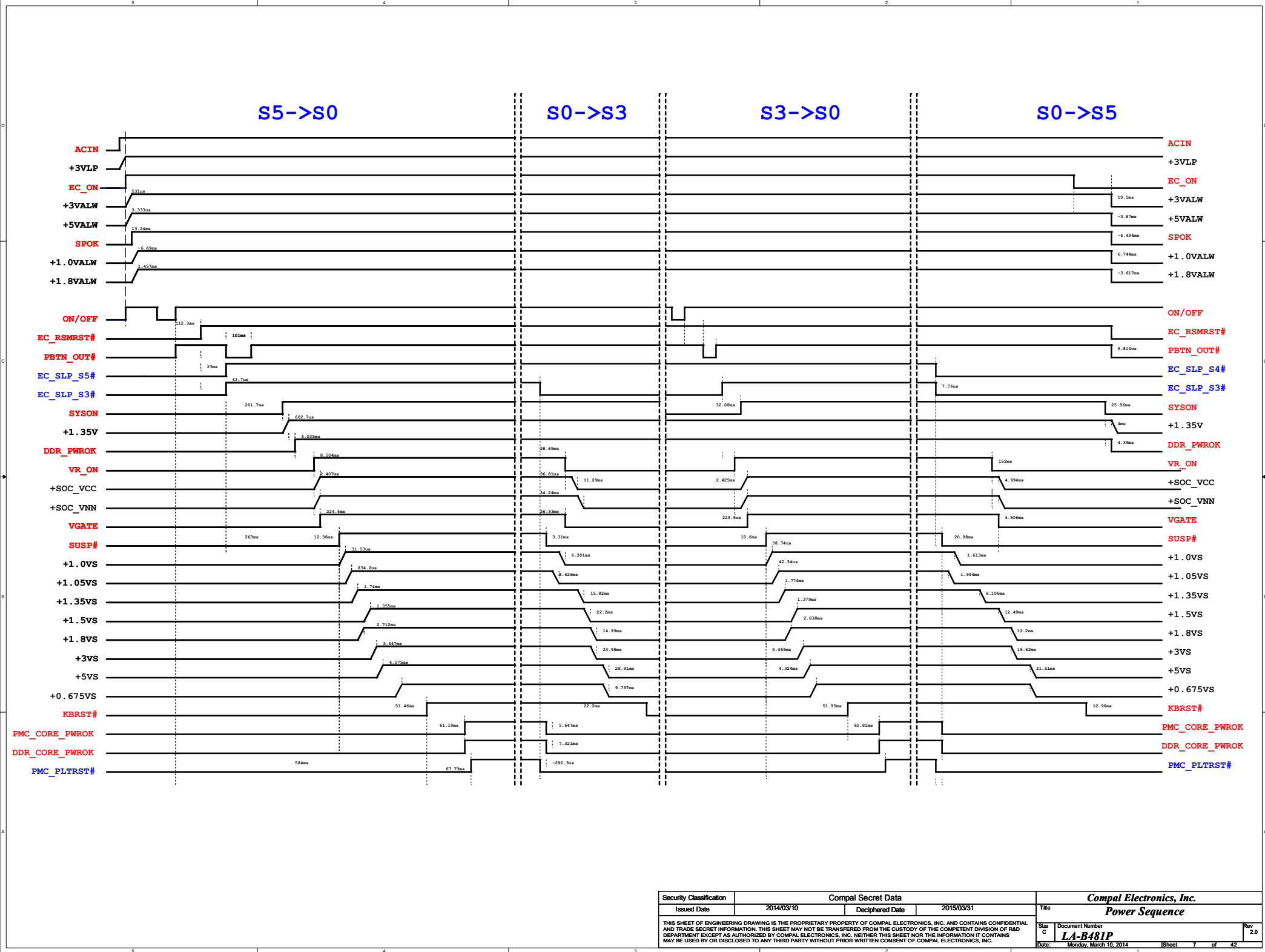
S5->S0

S0->S3

S3->S0

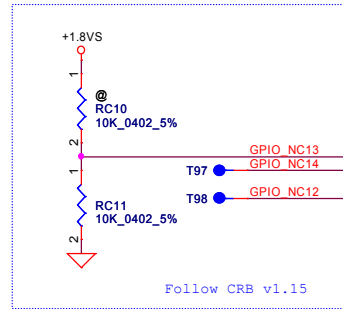
S0->S5





HDMI

Follow CRB v1.15 0ohm till to GND



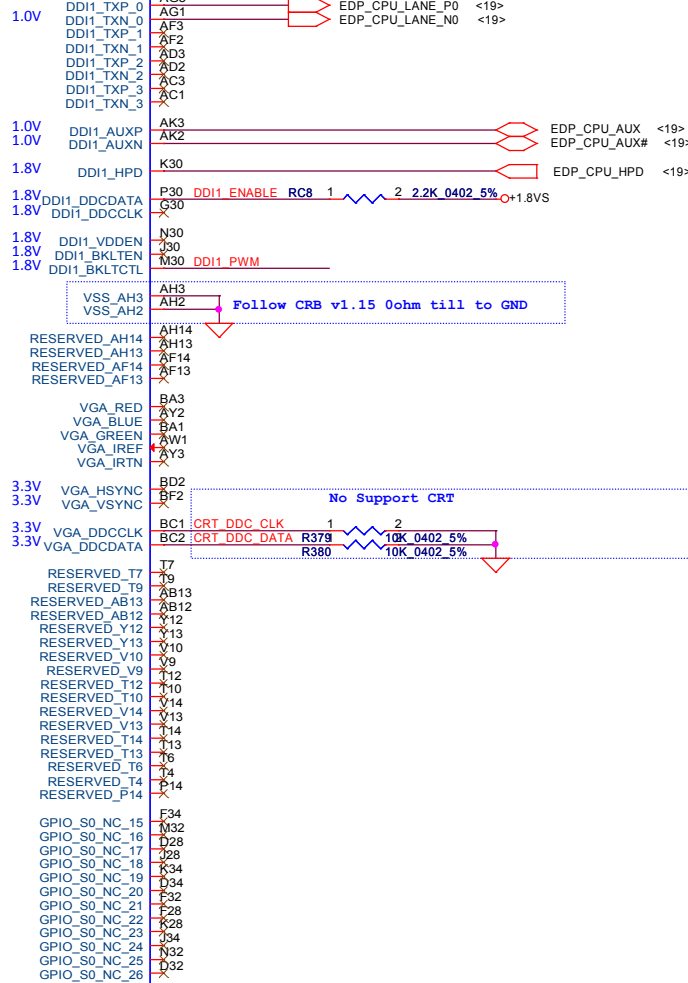
GPIO_S0_NC[13]:
Multiplexed with Hardware Straps Pin:MDSI_DDCDATA

USOC1C

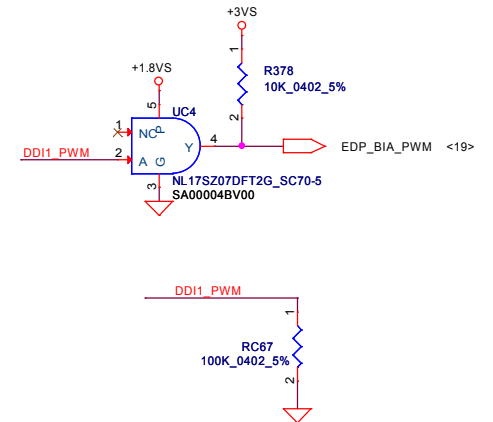
3 OF 10

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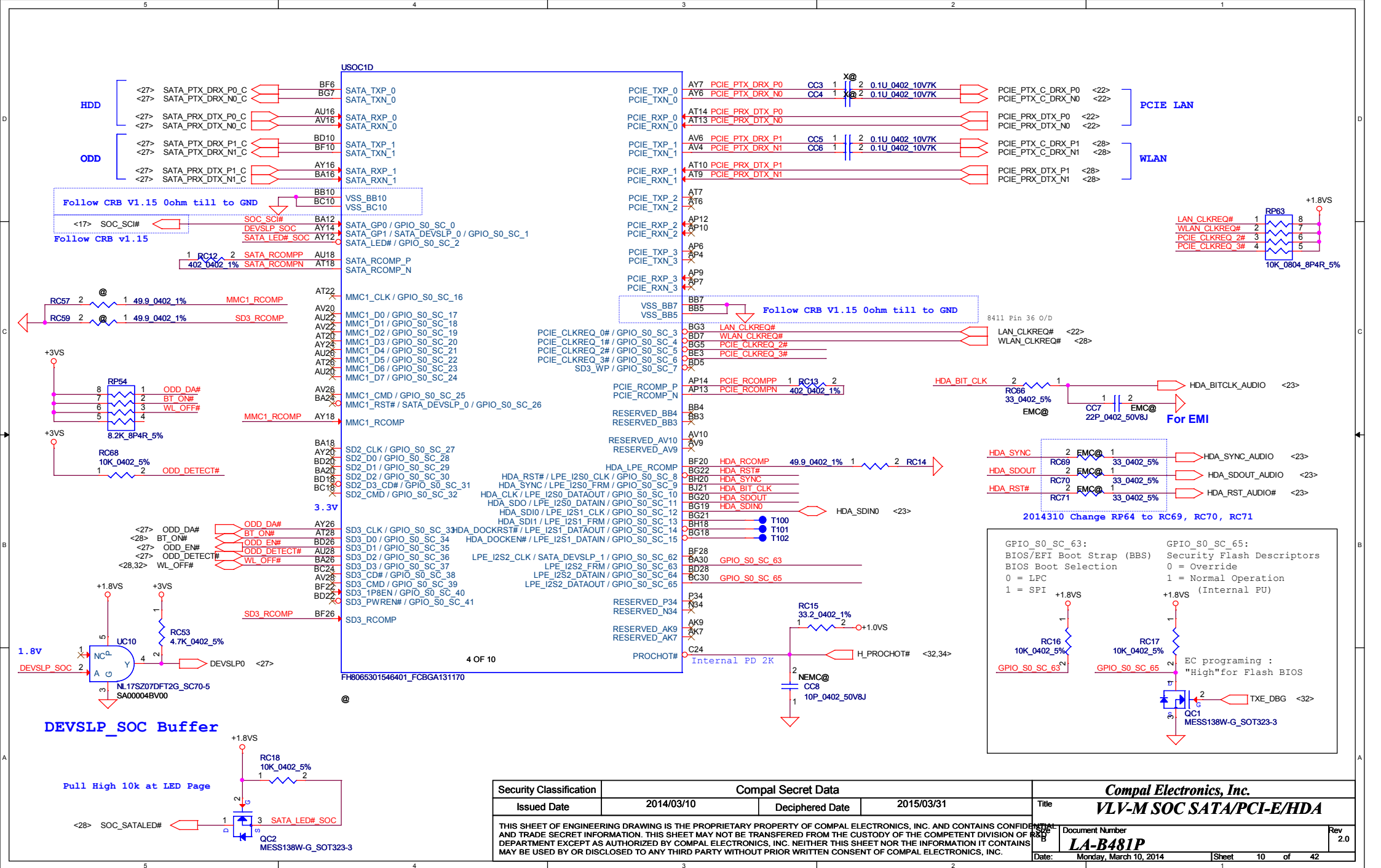
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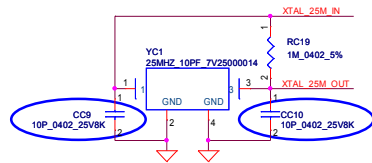


eDP to LVDS Panel



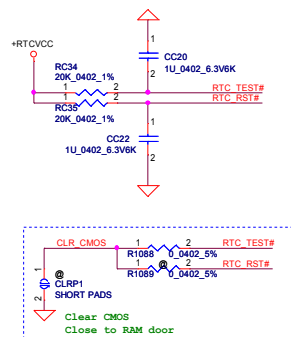
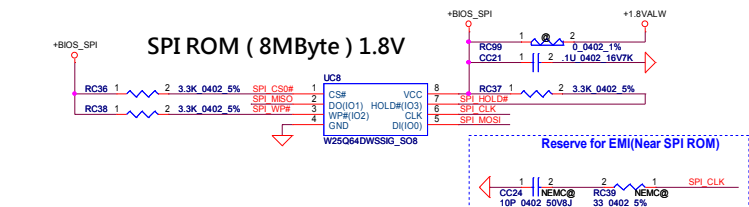
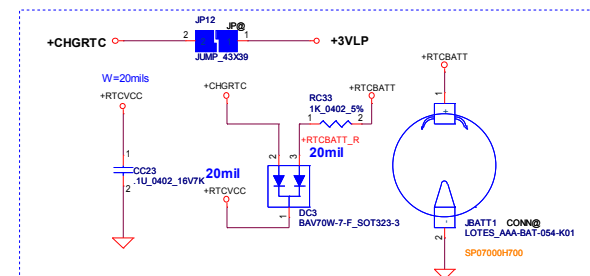
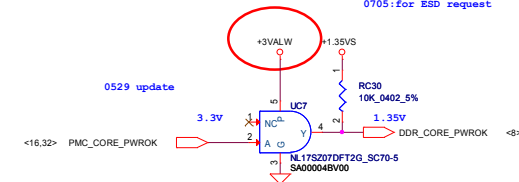
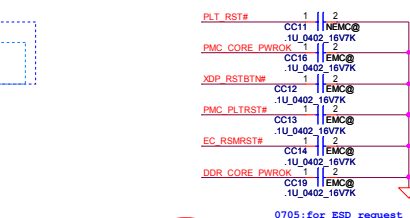
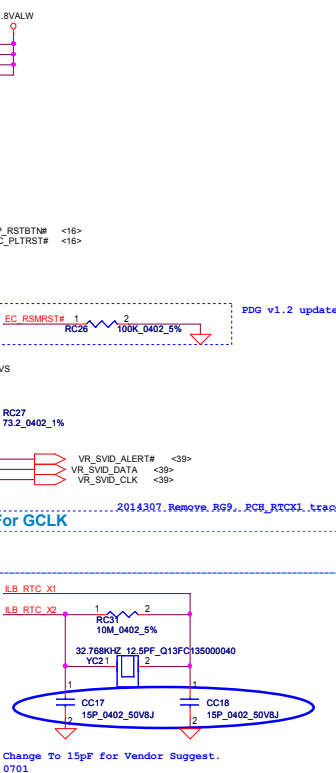
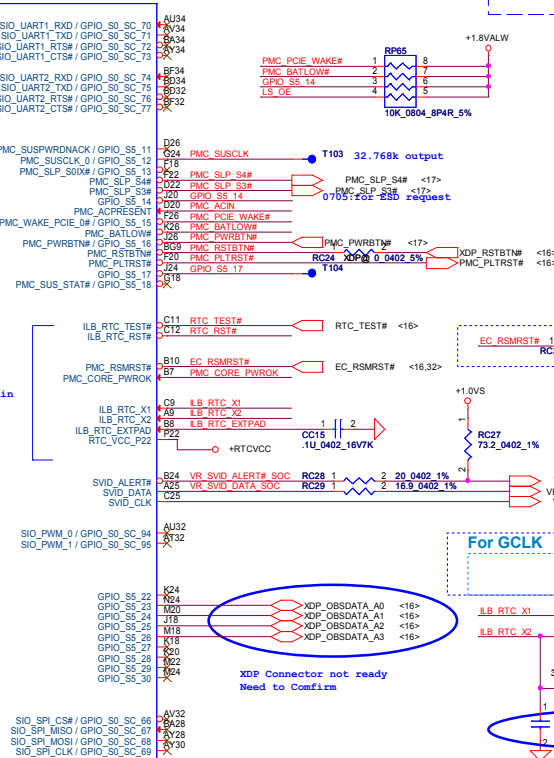
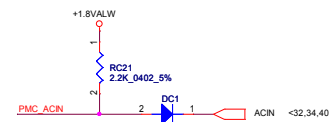
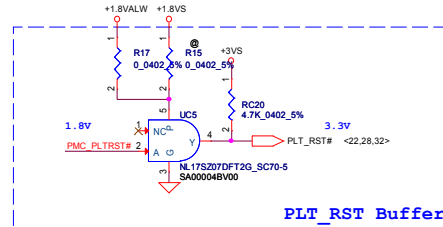
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2015/03/31		Title		VLV-M SOC Display	
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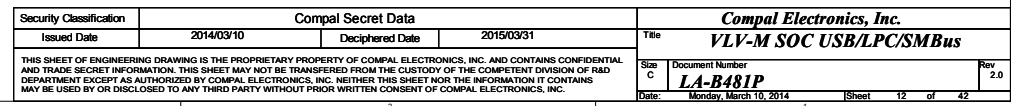


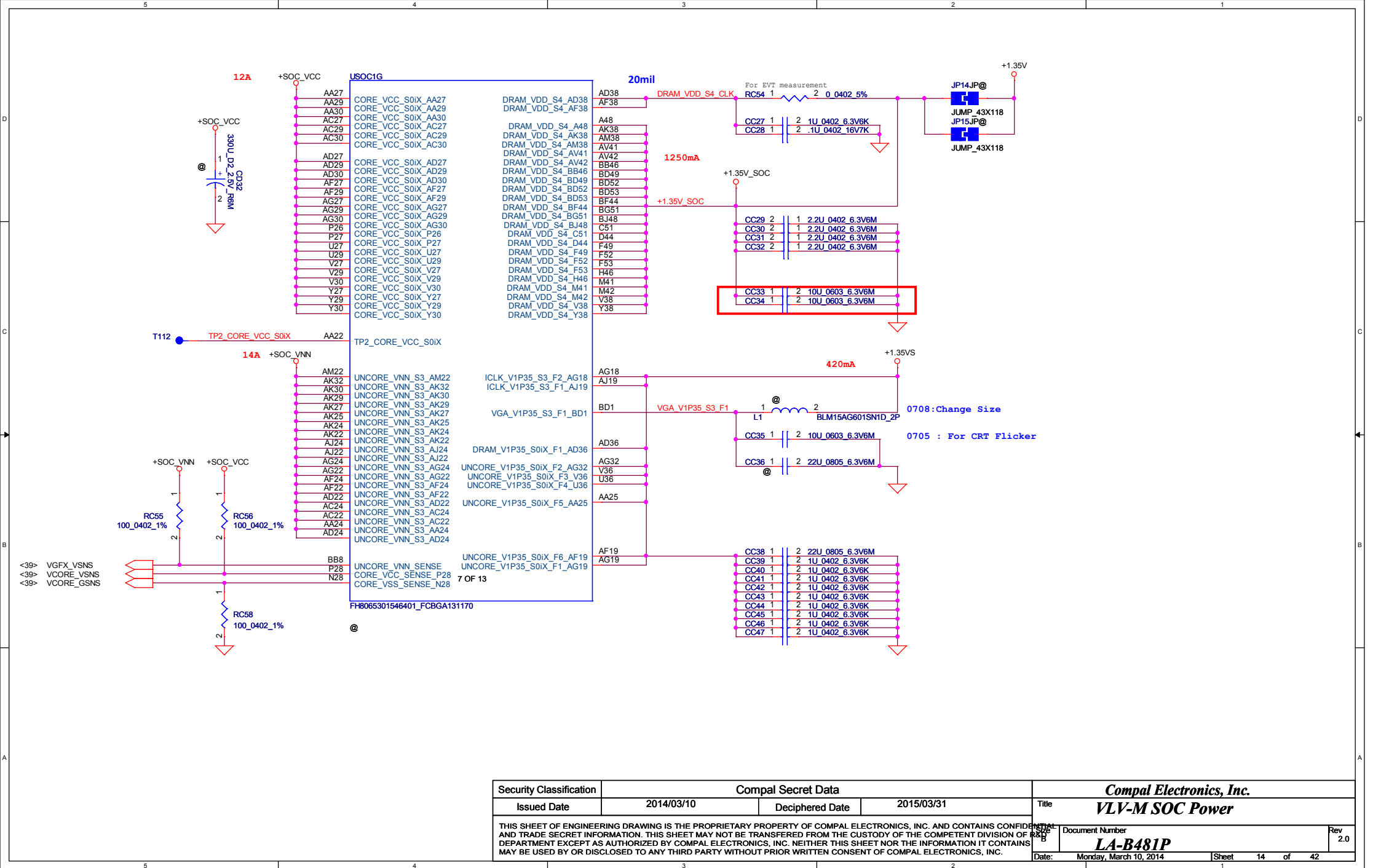
<31> PCH_X1

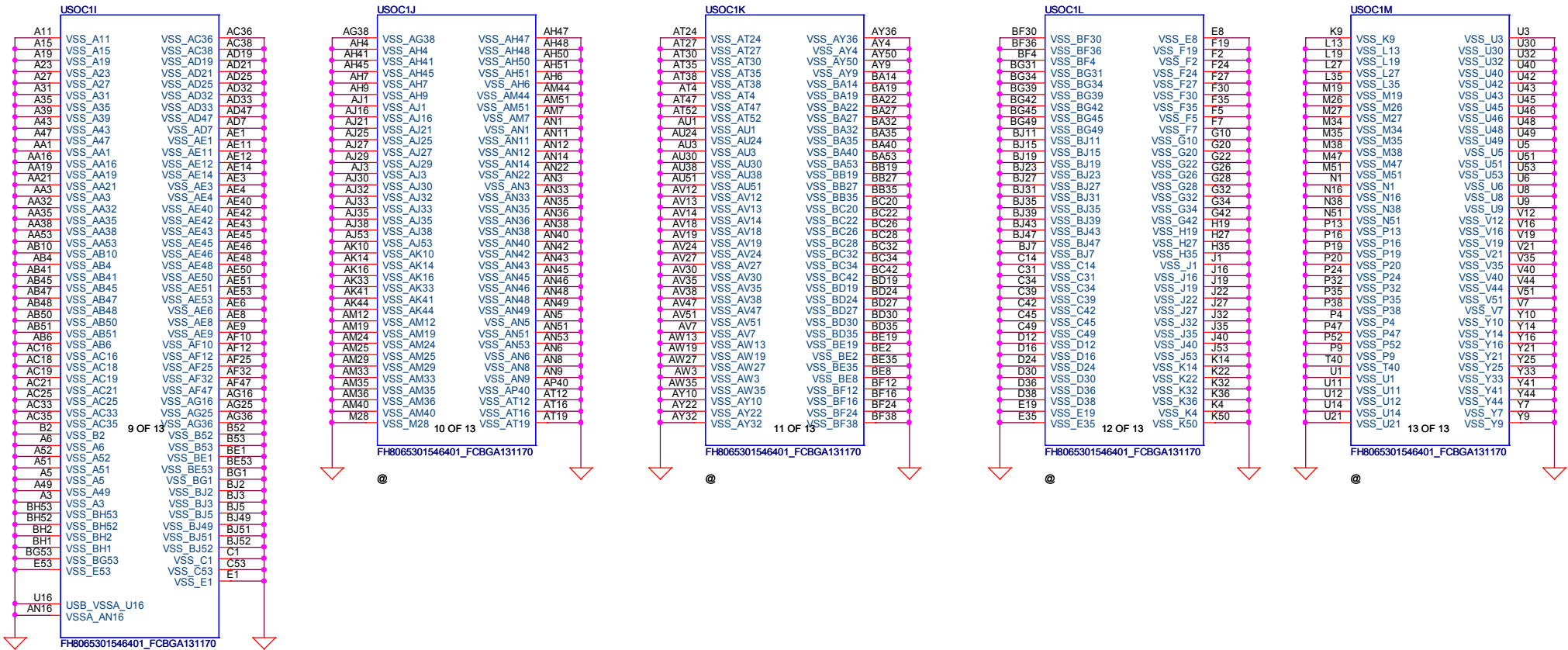
Diagram showing a signal path labeled PCH_X1. The path includes a component labeled RG10 and a connection point labeled GCLK@. The path continues to XTAL_25M_IN, which is associated with a value of 0_0402_5%.



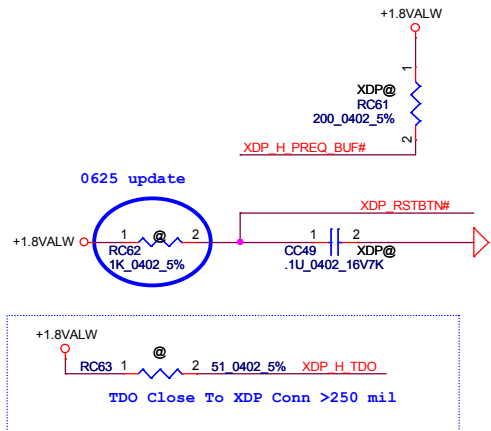
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Title		VLV-M SOC CLK/PMU/SPI			
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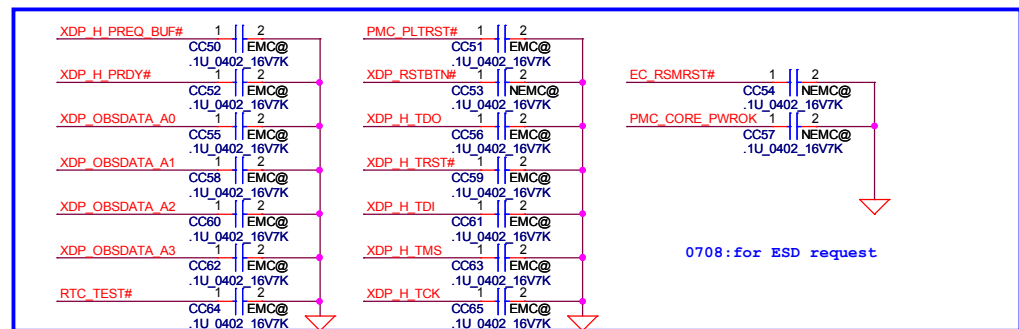
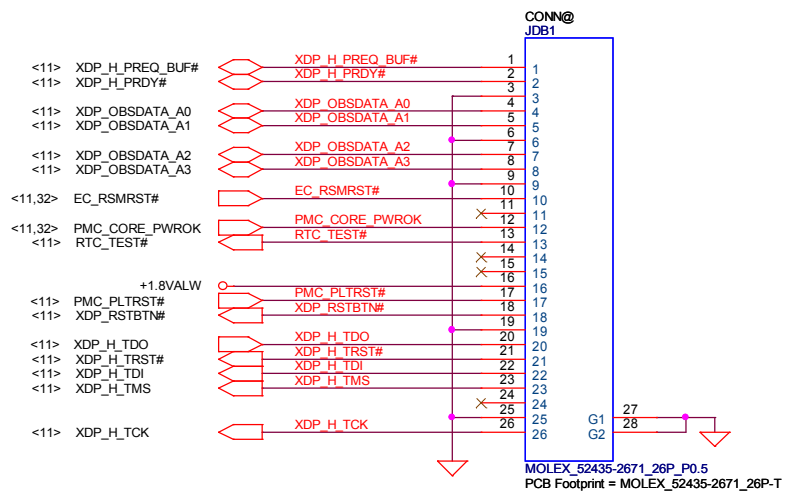




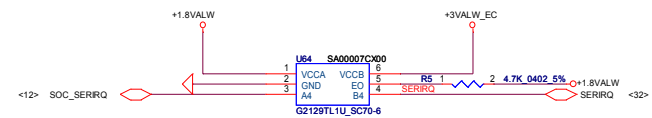
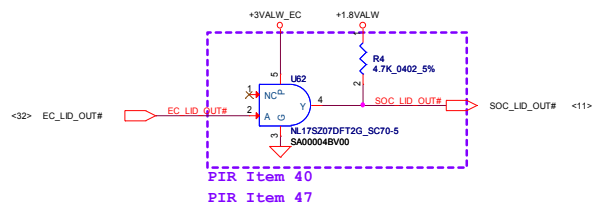
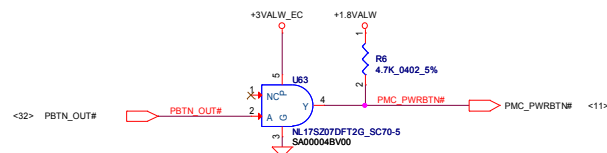
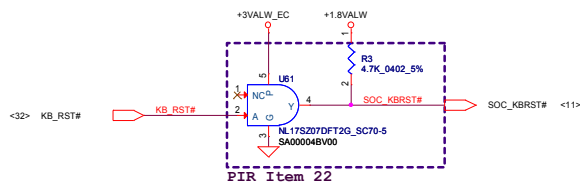
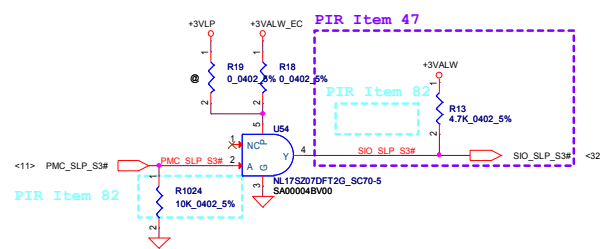
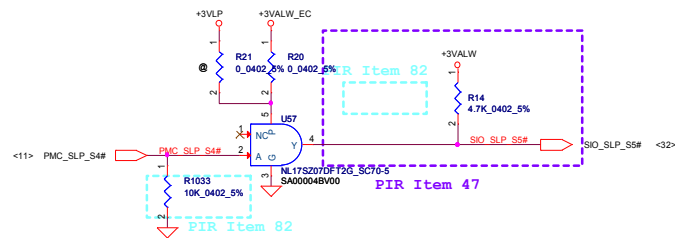
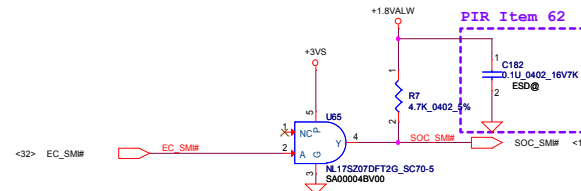
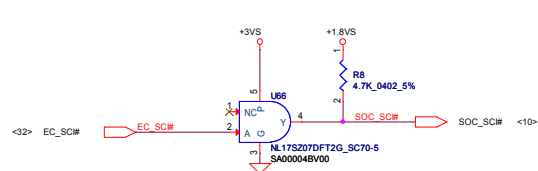
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XDP-SFF-26Pin



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				VLV-M SOC Debug	
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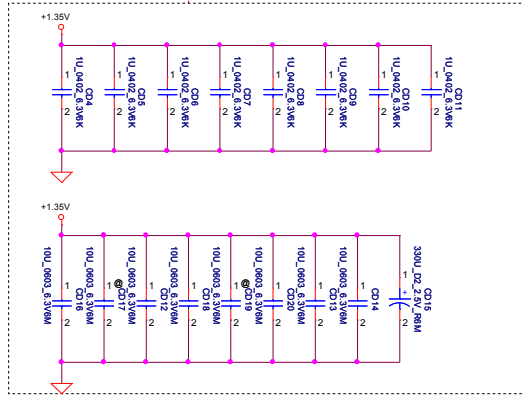
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Populate RD1, De-Populate RD7 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3

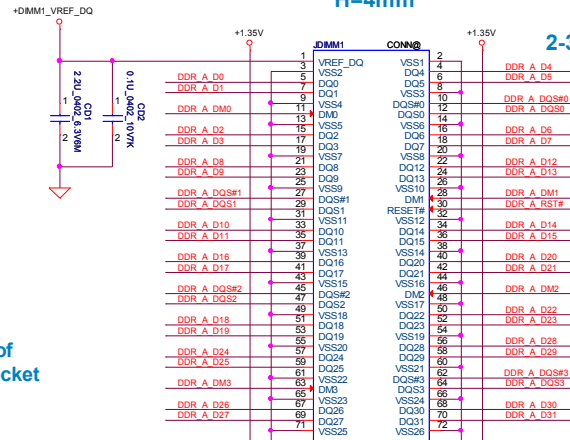
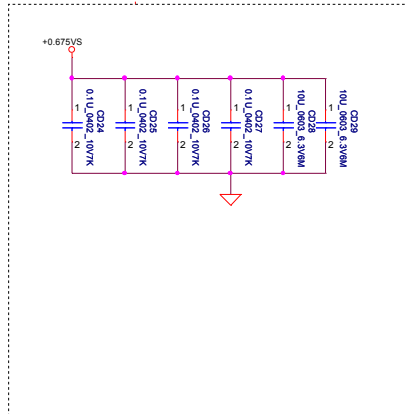
<> DDR_A_DM[0..7]
<> DDR_A_DQS[0..7]
<> DDR_A_DQ[0..63]
<> DDR_A_DQS[0..7]
<> DDR_A_MA[0..15]

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

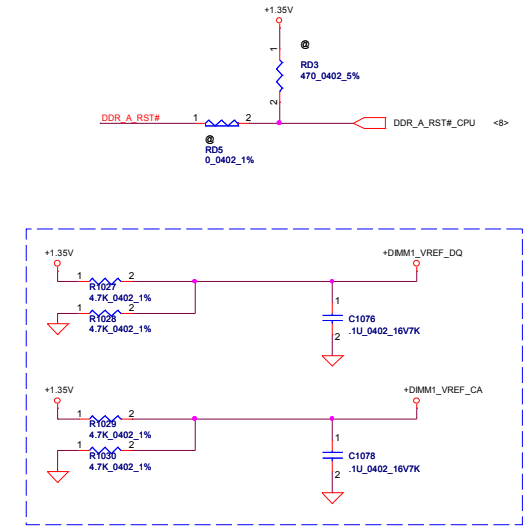


Layout Note:
Place near JDIMM1.203,204



2-3A to 1 DIMMs/channel

CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN



M_ODT0 1 2 DDR_A_ODT0
M_ODT1 1 2 DDR_A_ODT1
R09 0.0402_1%

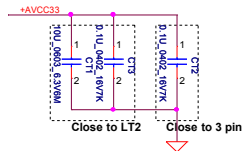
Need to Confirm

Channel A

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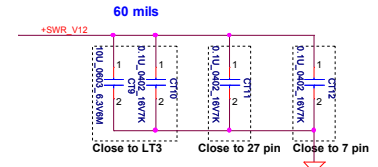
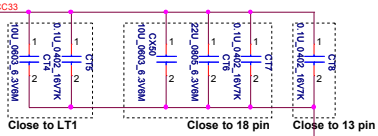


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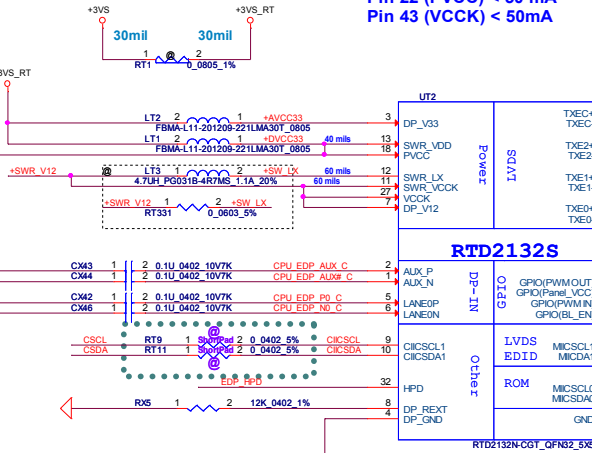
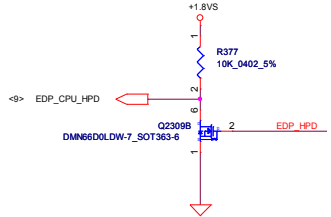
Power Consumption:

Pin22 (DPV33) < 20mA
 Pin 11 (DP_V12) < 100mA
 Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
 Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 22 (PVCC) < 50 mA
 Pin 43 (VCCK) < 50mA



<9> EDP_CPU_AUX
 EDP_CPU_AUX#
 <9> EDP_CPU_LANE_P0
 EDP_CPU_LANE_N0

EDP_CPU_AUX
 EDP_CPU_AUX#
 EDP_CPU_LANE_P0
 EDP_CPU_LANE_N0

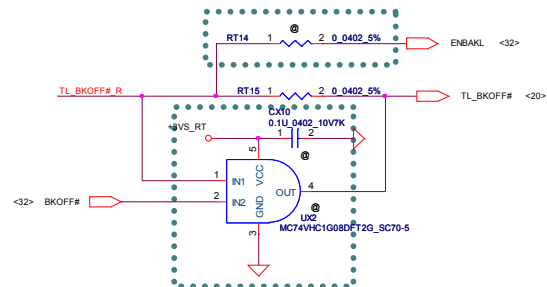


RTD2132R : SA000069200
 RTD2132N : SA00007A300

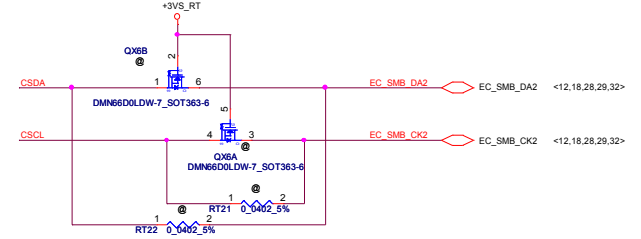
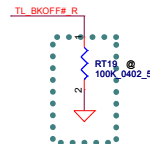
1: RevD W EEPROM
 0: RevE W/O EEPROM

		Pin47 MIIC_SDA	
		0	1
Pin48 MIIC_SCL	0	x	EP MODE
	1	ROM	EEPROM

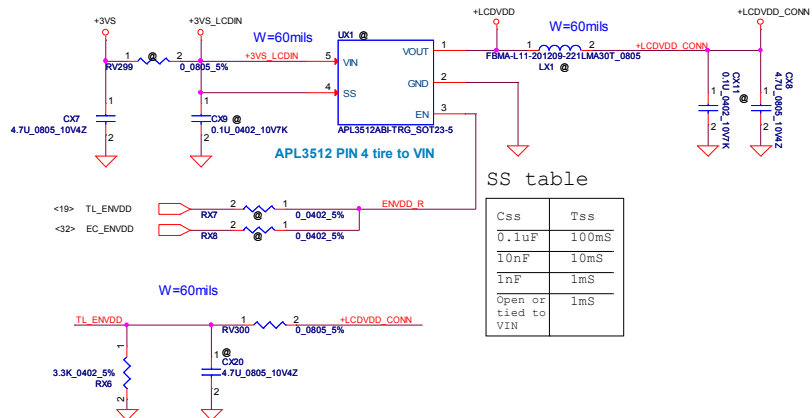
Vendor advise reserve it



Pull-Down 100K

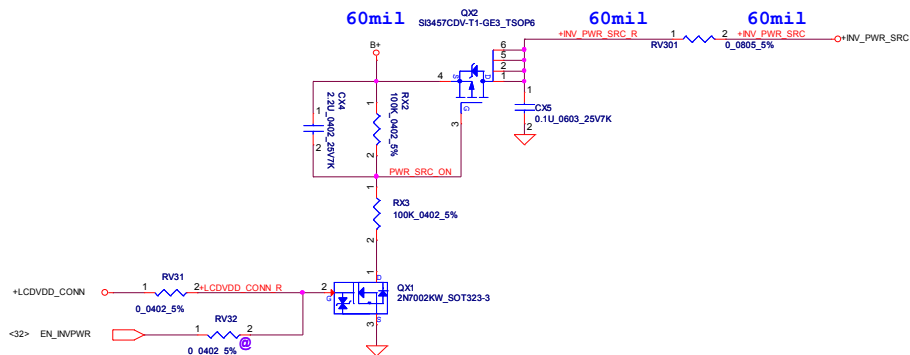


LCD PWR CTRL

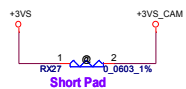


Css	Tss
0.1 μ F	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

LCD backlight PWR CTRL

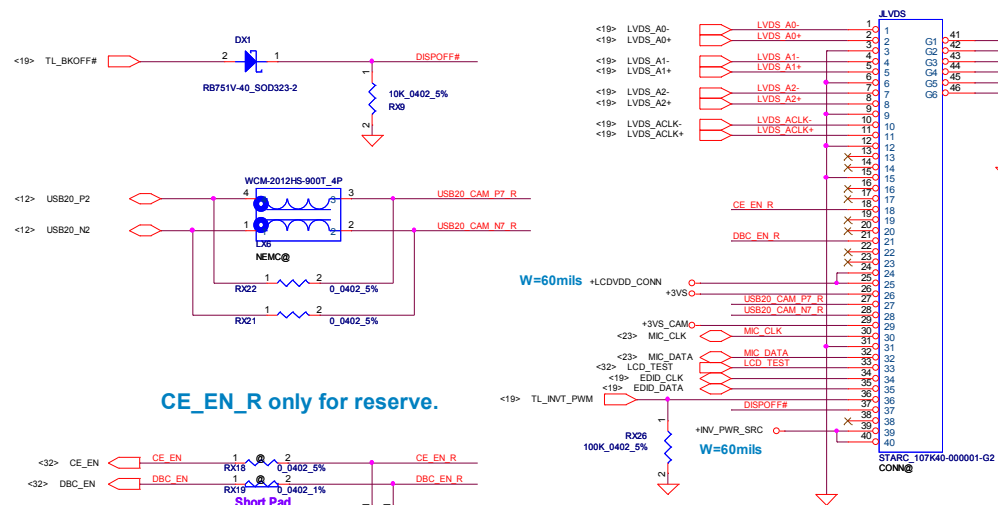


Webcam PWR CTRL

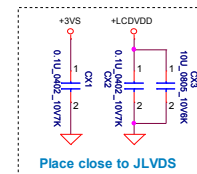
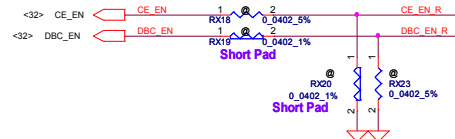


Short pad list
RX19
RX27

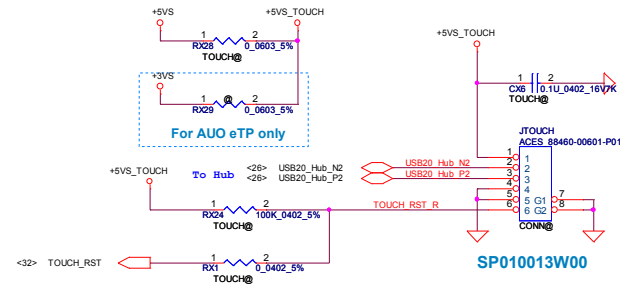
LVDS Connector



CE_EN_R only for reserve.

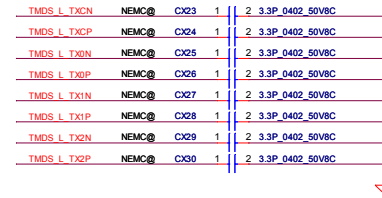
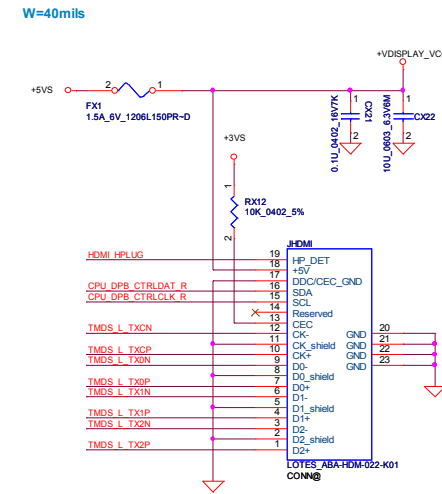
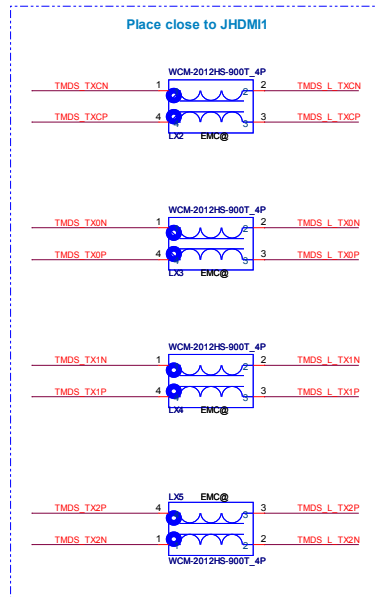
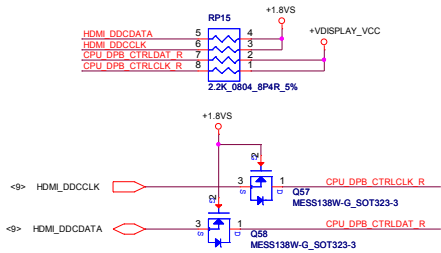
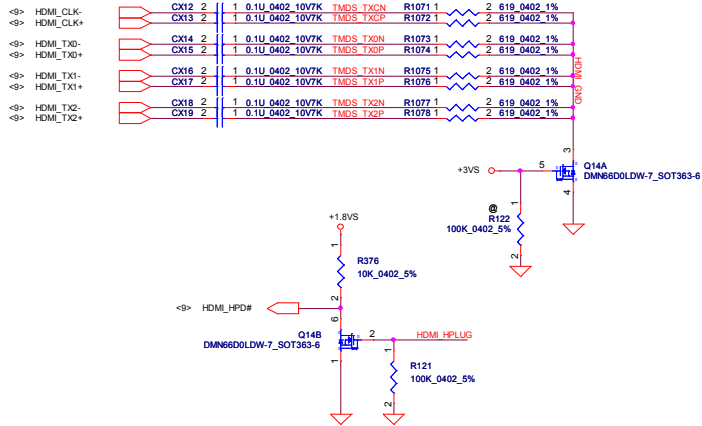


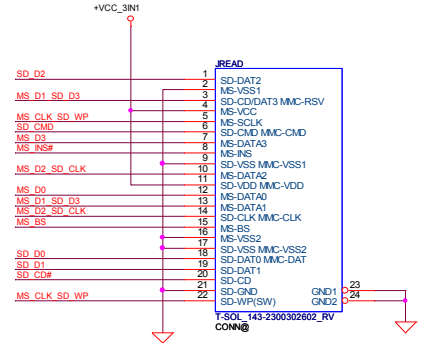
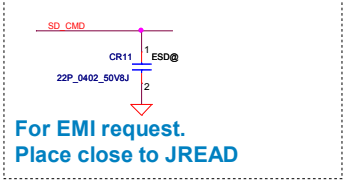
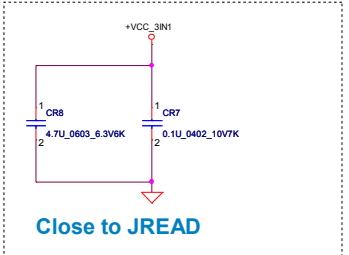
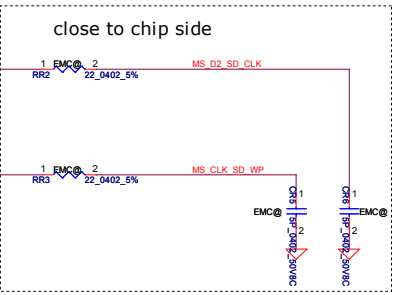
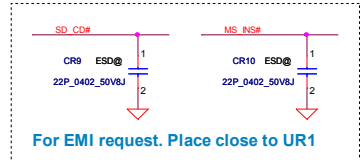
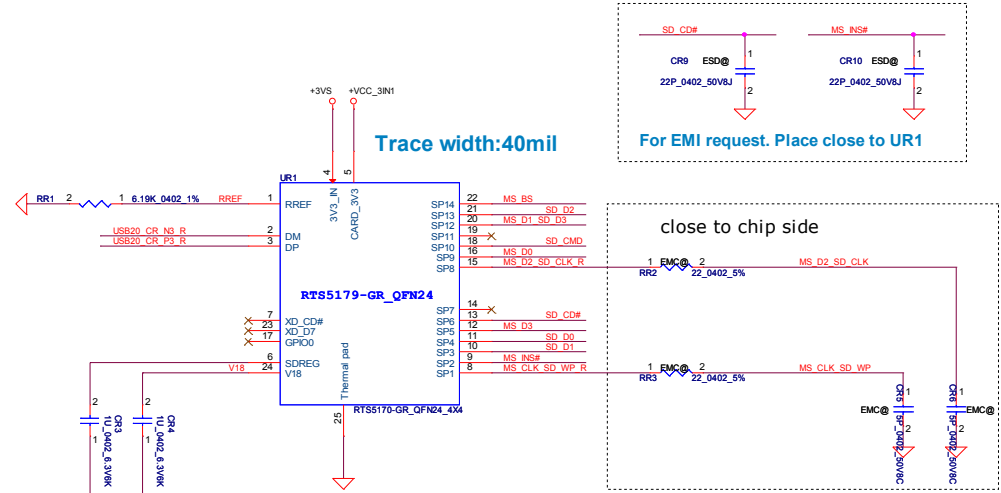
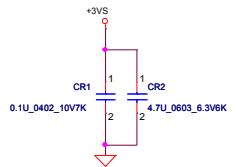
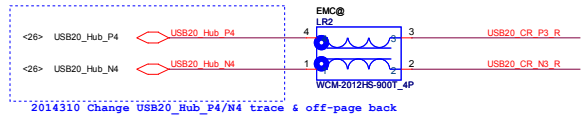
*** Touch Screen Panel**

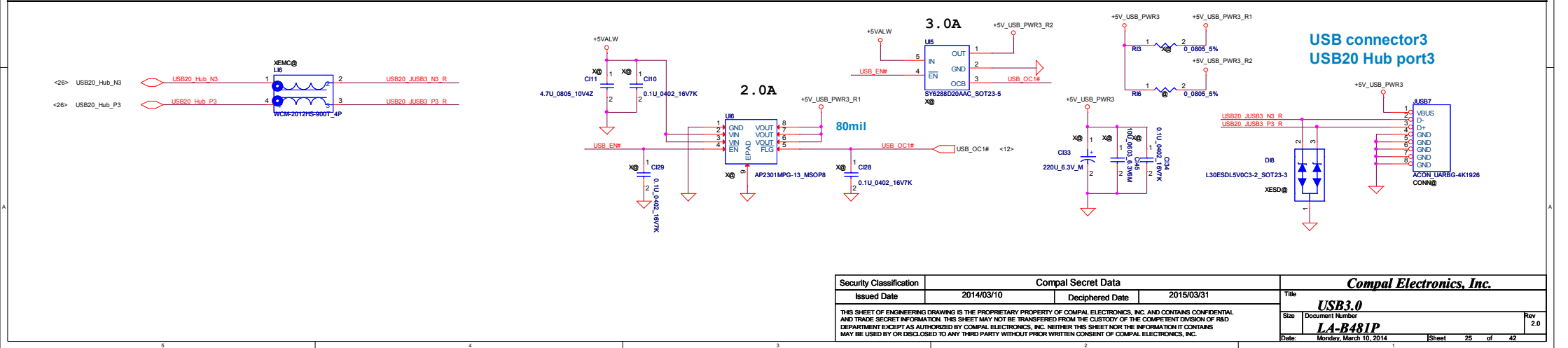
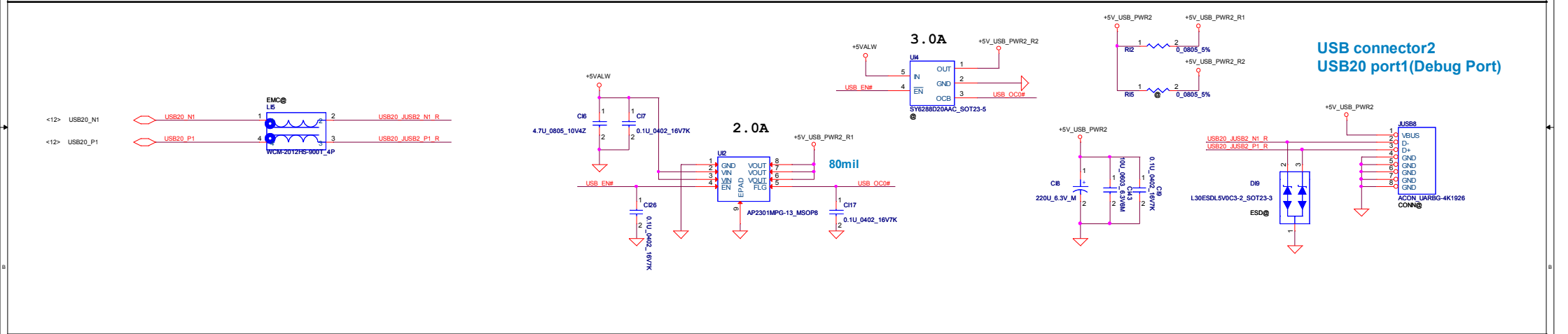
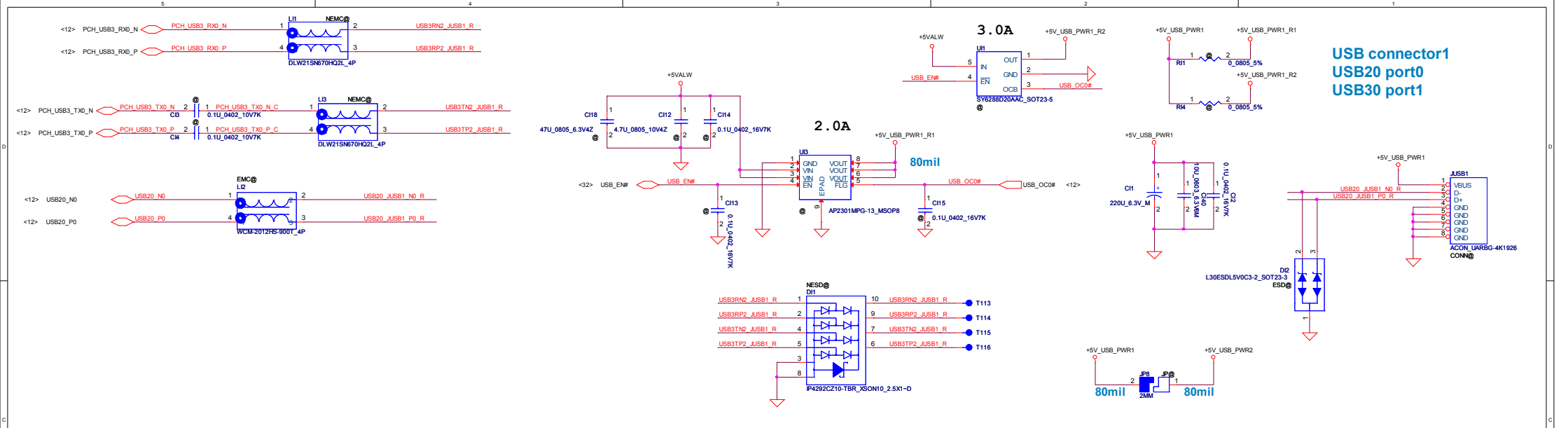


OAK 15 only

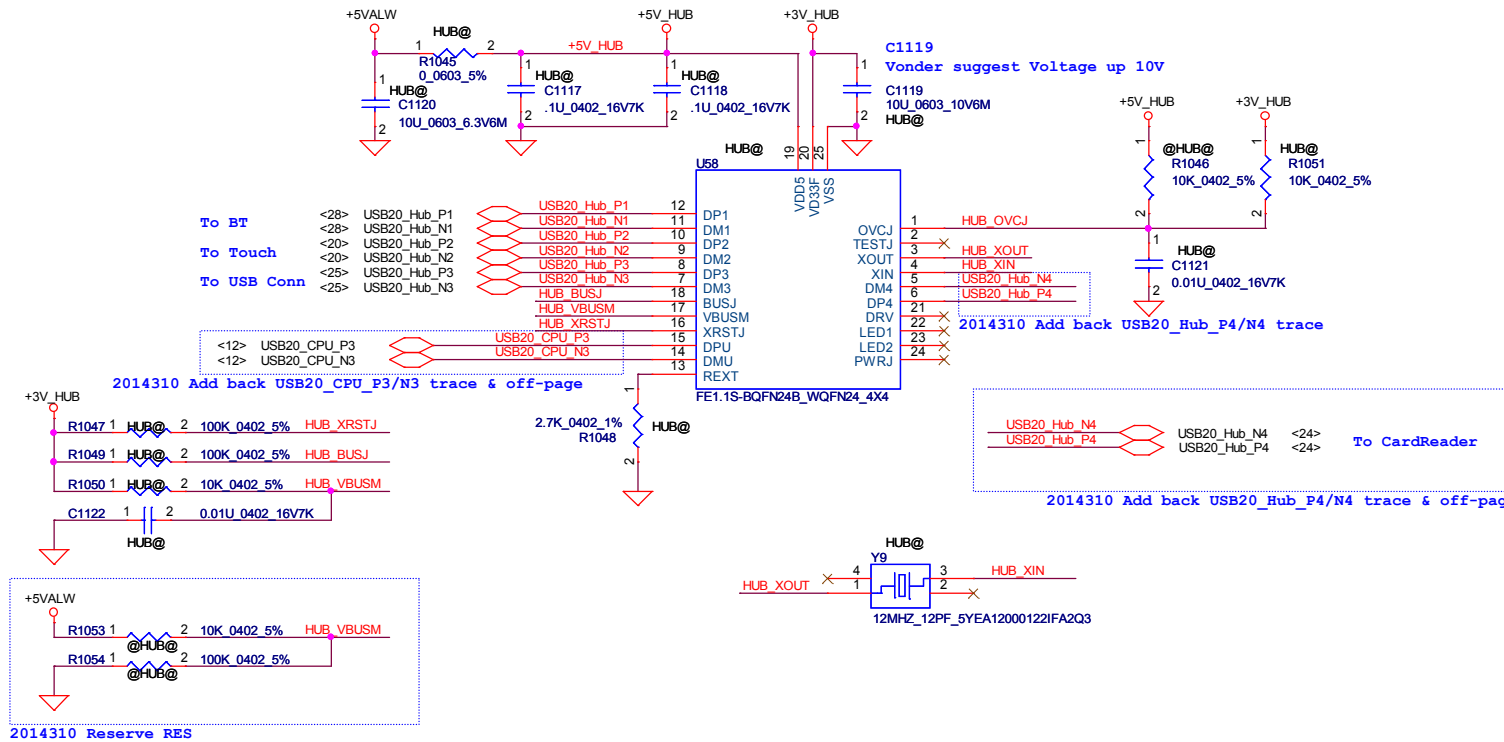
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Issued Date	2014/03/10	Deciphered Date	2015/03/31	Title		
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				Size	Document Number	Rev
				<i>LA-B481P</i>		2.0
Date: Monday, March 10, 2014				Sheet	20	of 42







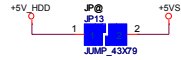
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				Rev	2.0
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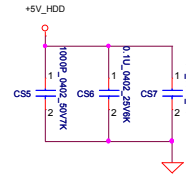
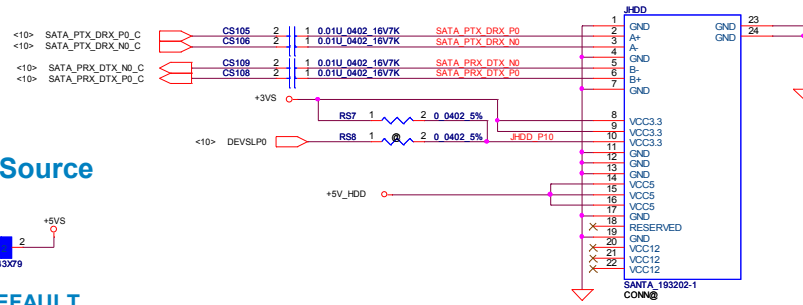
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Date: Monday, March 10, 2014				Sheet	26 of 42

SATA HDD Connector

+5V_HDD Source

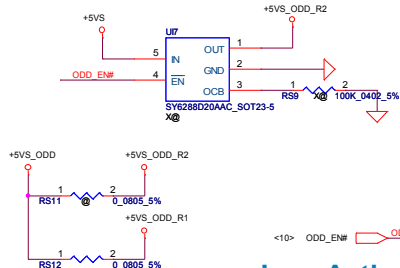


SHORT DEFAULT

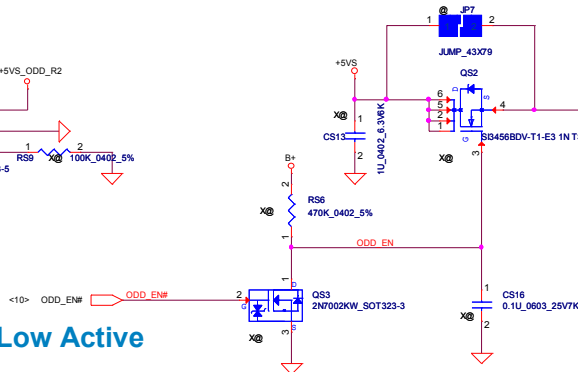


ODD Power Control

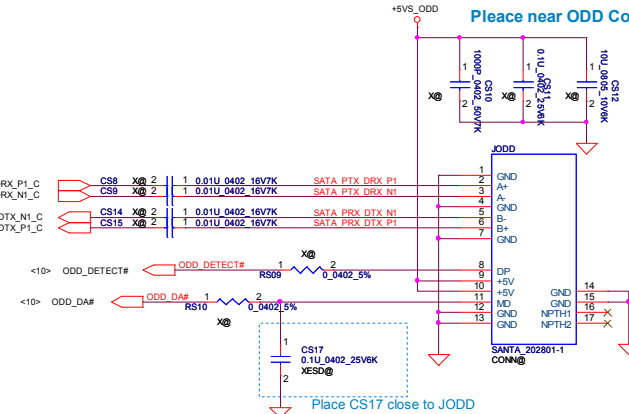
SATA ODD Connector



Low Active

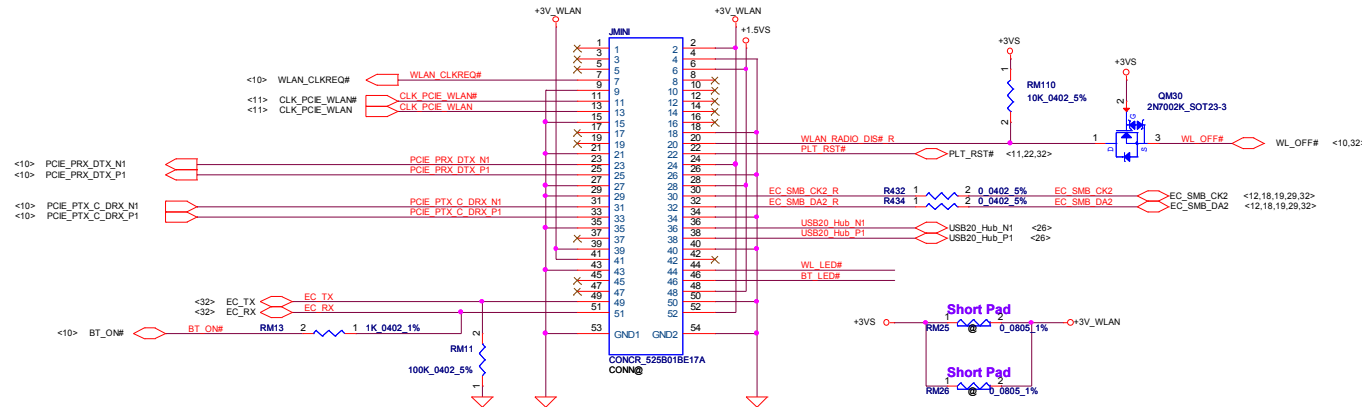


Place near ODD Connector



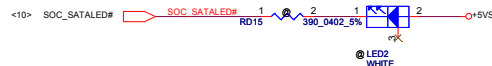
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/10	Deciphered Date	2015/03/31	Title	HDD/ODD
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				Date	Monday, March 10, 2014
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Mini WLAN/WIMAX H=6.7



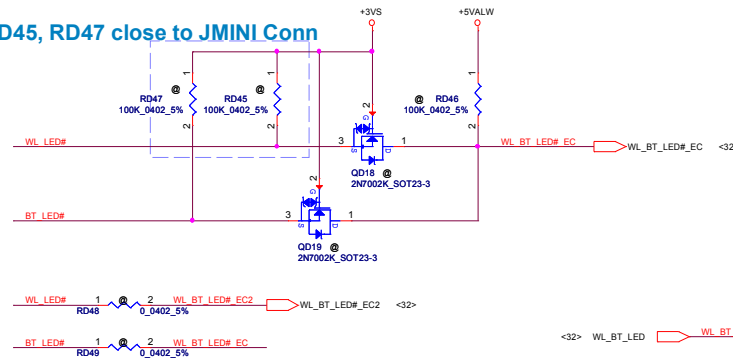
10mils, All pins

HDD LED



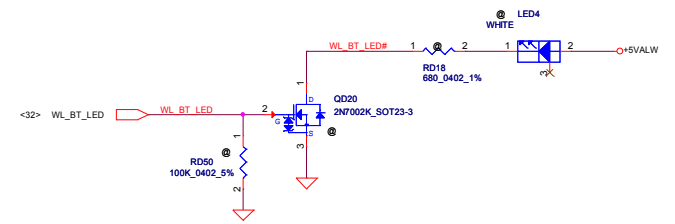
12-21C-T3D-CM2P1B18X-2C_WHITE

RD45, RD47 close to JMIN Conn



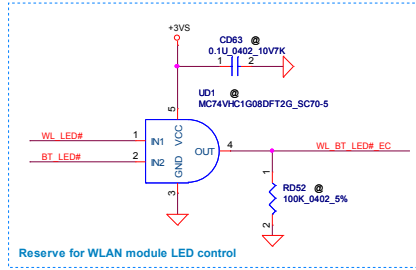
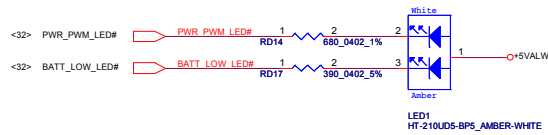
Reserve for WLAN module modified

Wireless LED



Reserve for WLAN module modified

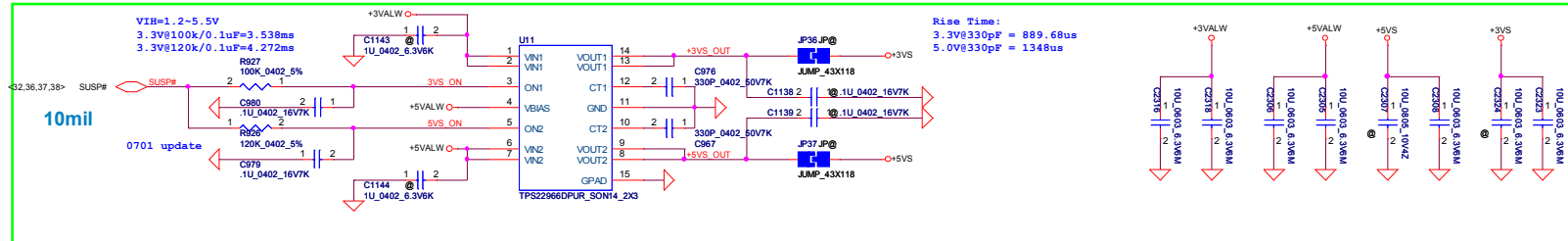
Power / Battery LED



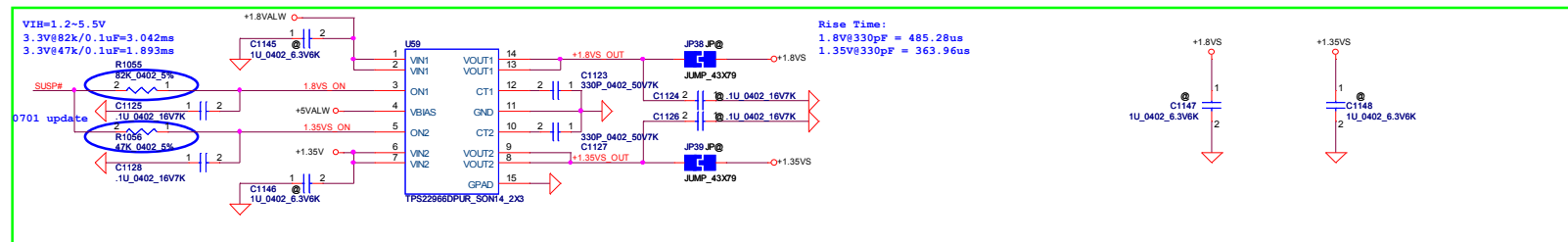
Reserve for WLAN module LED control

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				Size	Document Number	Rev
				L4-B481P		2.0
				Date:	Monday, March 10, 2014	Sheet 28 of 42

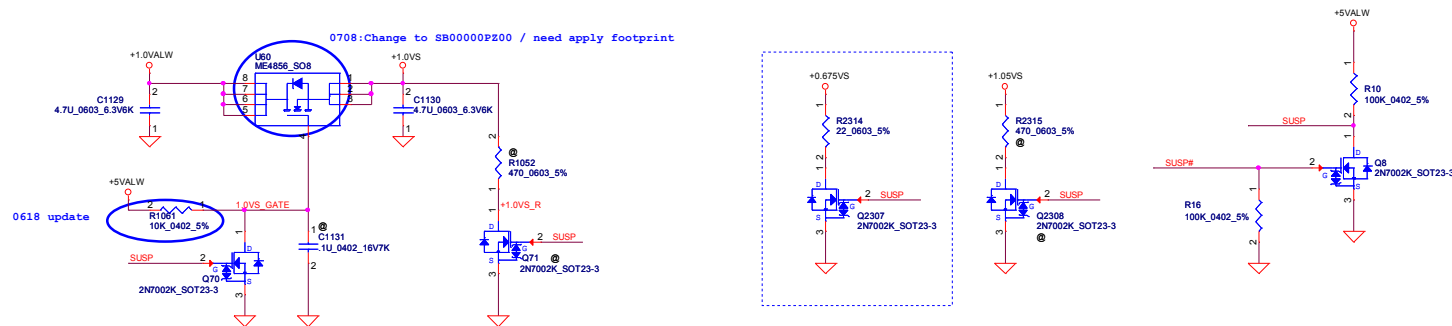
+5VS and +3VS Switch



+1.8VS and +1.35VS Switch



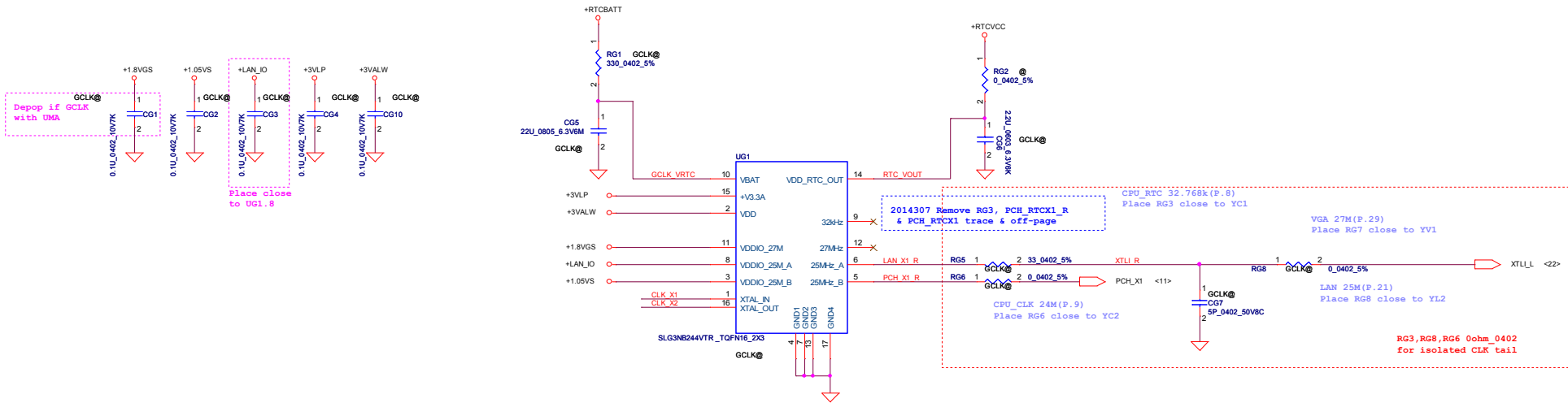
+1.0VALW TO +1.0VS

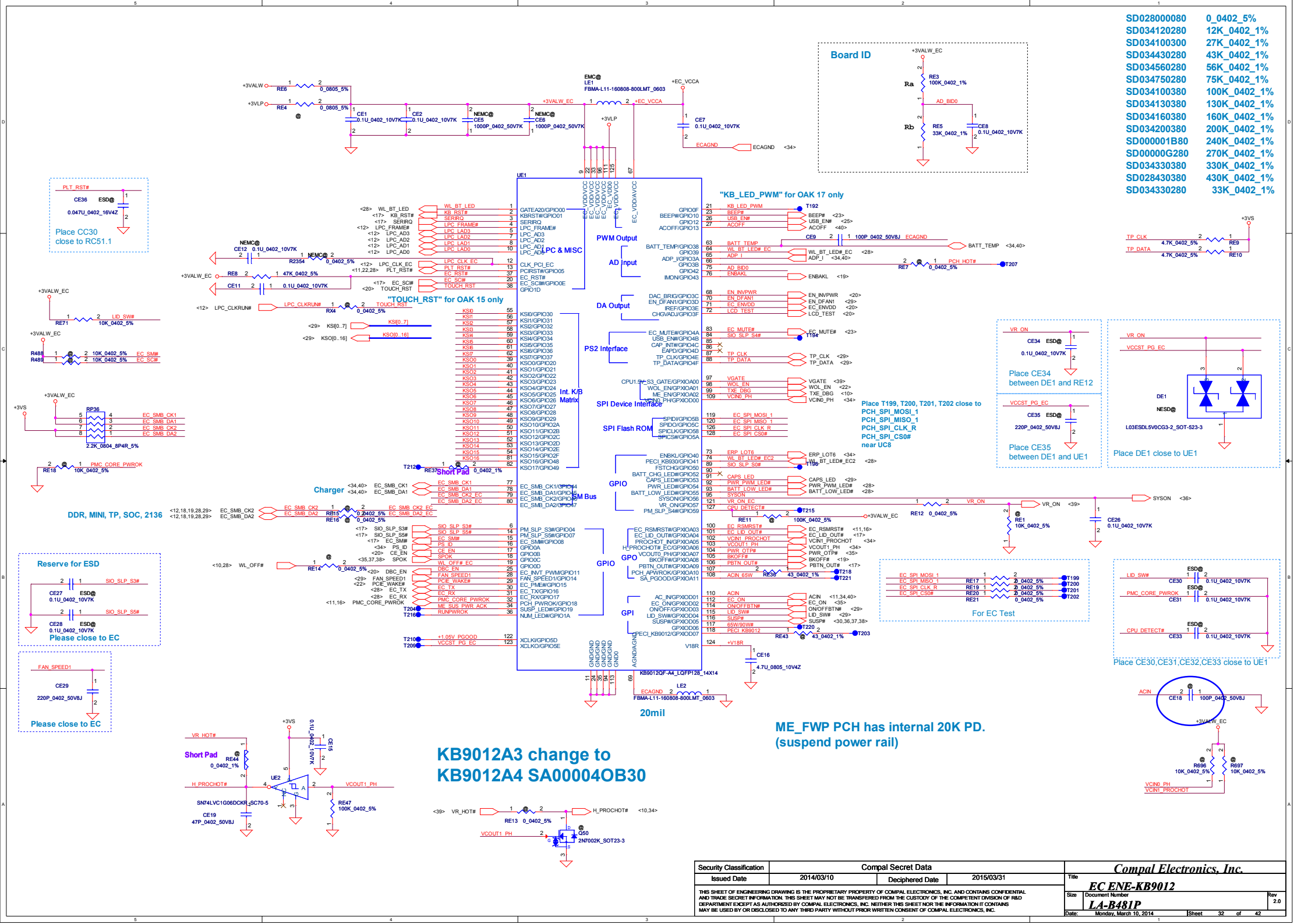


For Intel S3 Power Reduction

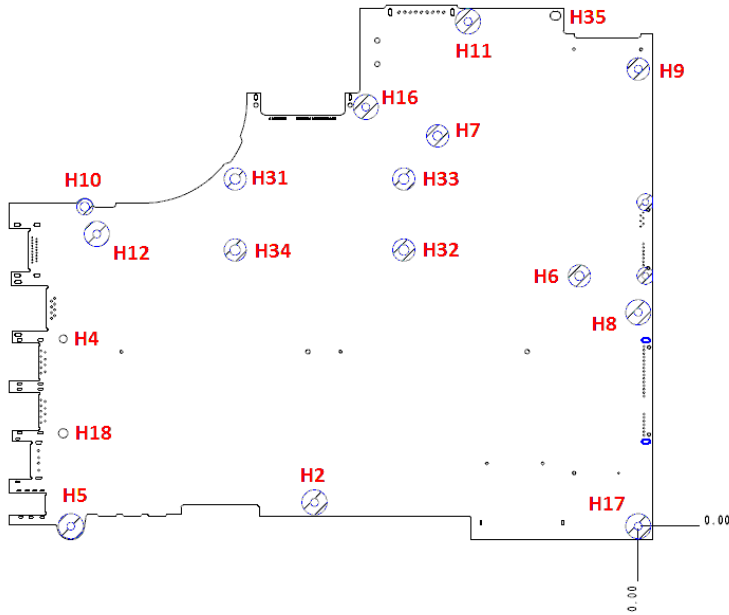
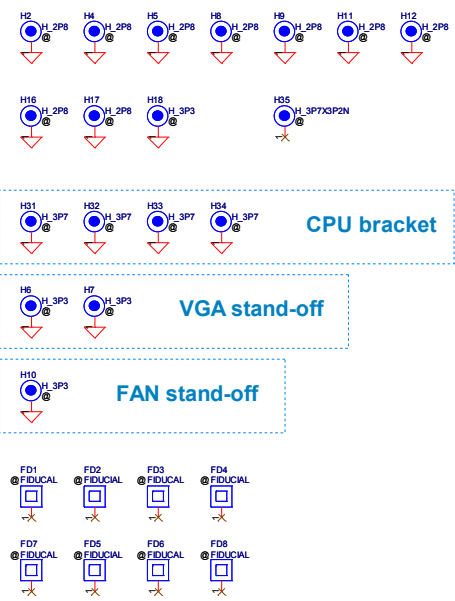
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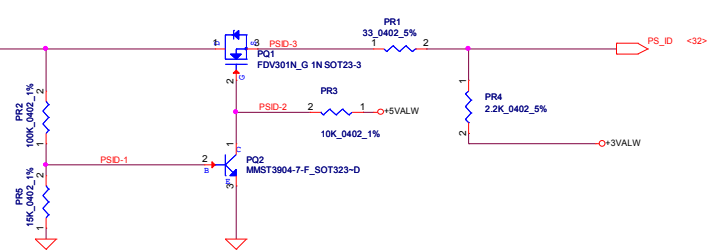
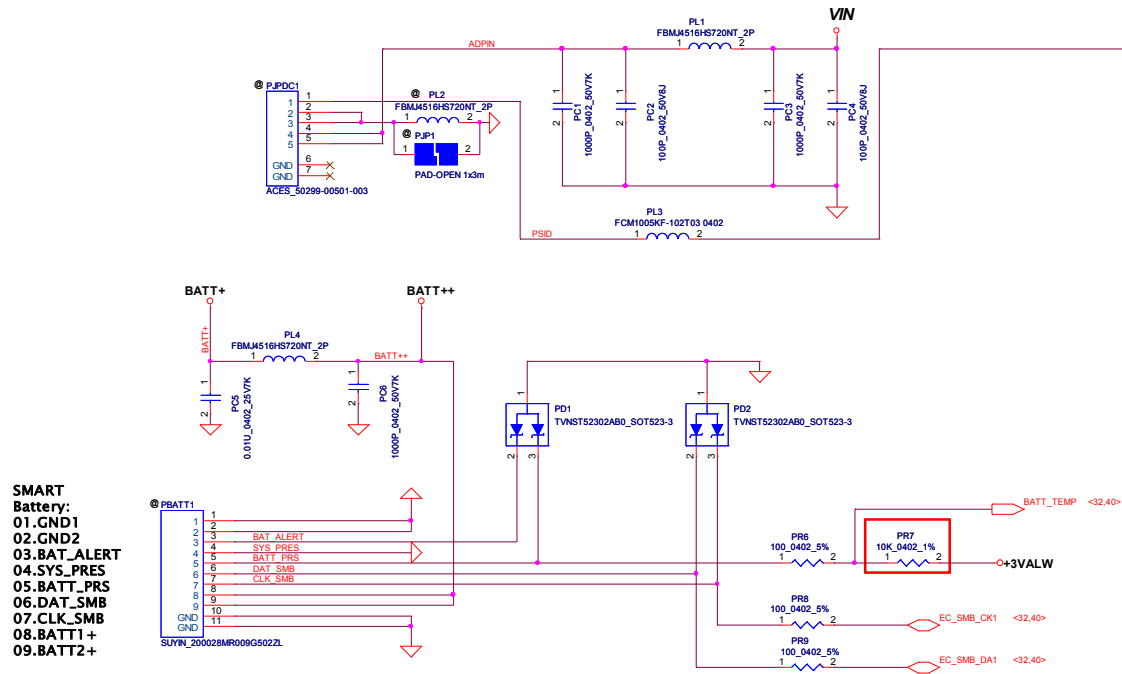
SLG3NB3374VTR is for DIS by output 24M*1,25M*1, 27M*1, 32K*1
SLG3NB3375VTR is for UMA by output 24M*1, 25M*1, 32K*1
SLG3NB244VTR is for UMA by output 25M*2, 32K*1



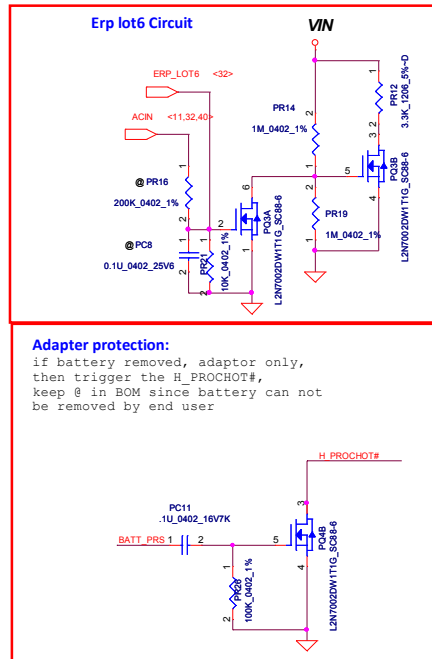


Screw Hole

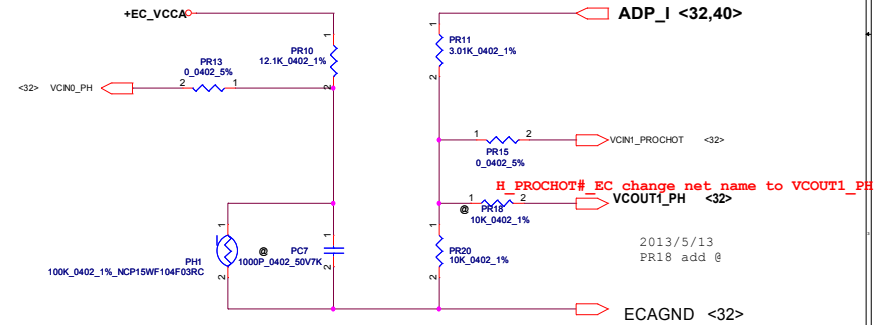
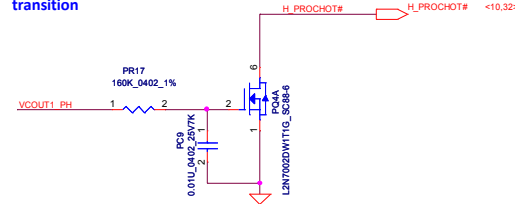




Other component (37.1)



Delay adaptor OC H_PROCHOT#
2ms while hybrid power
transition



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Date:	Monday, March 10, 2014	Sheet	34	of	42

3VALWP
TDC 4.5A
Peak Current 7.09A
OCP current 8.51A

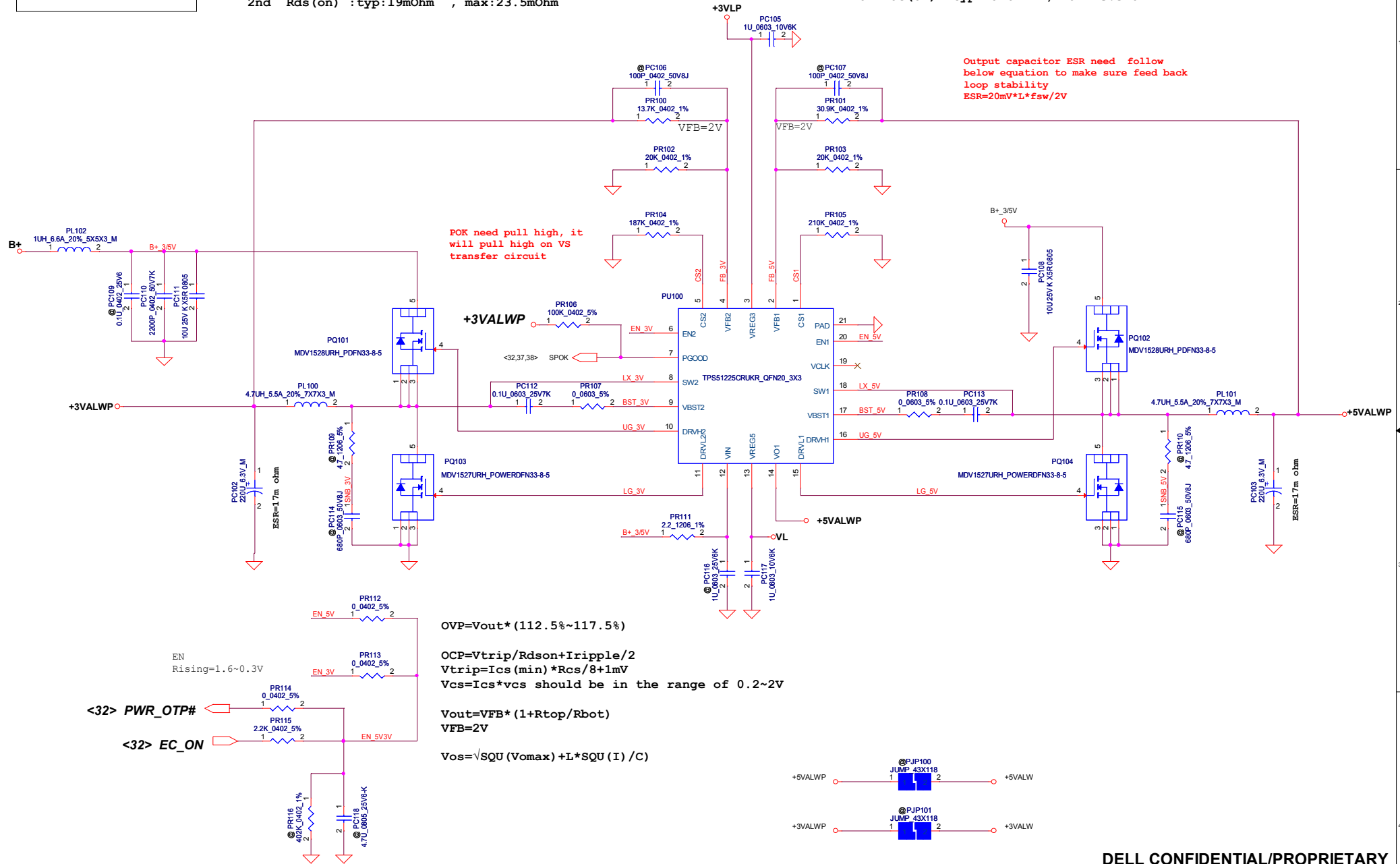
H/S main Rds(on) : typ:23.2mOhm, max:27.8mOhm
2nd Rds(on) : typ:27mOhm, max:34mOhm

L/S main Rds(on) : typ:19.7mOhm, max:23.7mOhm
2nd Rds(on) : typ:19mOhm, max:23.5mOhm

H/S main Rds(on) : typ:23.2mOhm, max:27.8mOhm
2nd Rds(on) : typ:27mOhm, max:34mOhm

L/S main Rds(on) : typ:19.7mOhm, max:23.7mOhm
2nd Rds(on) : typ:19mOhm, max:23.5mOhm

5VALWP
TDC 4.91A
Peak Current 8.63A
OCP current 10.36A



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				Date	Monday, March 10, 2014	Sheet 35 of 42

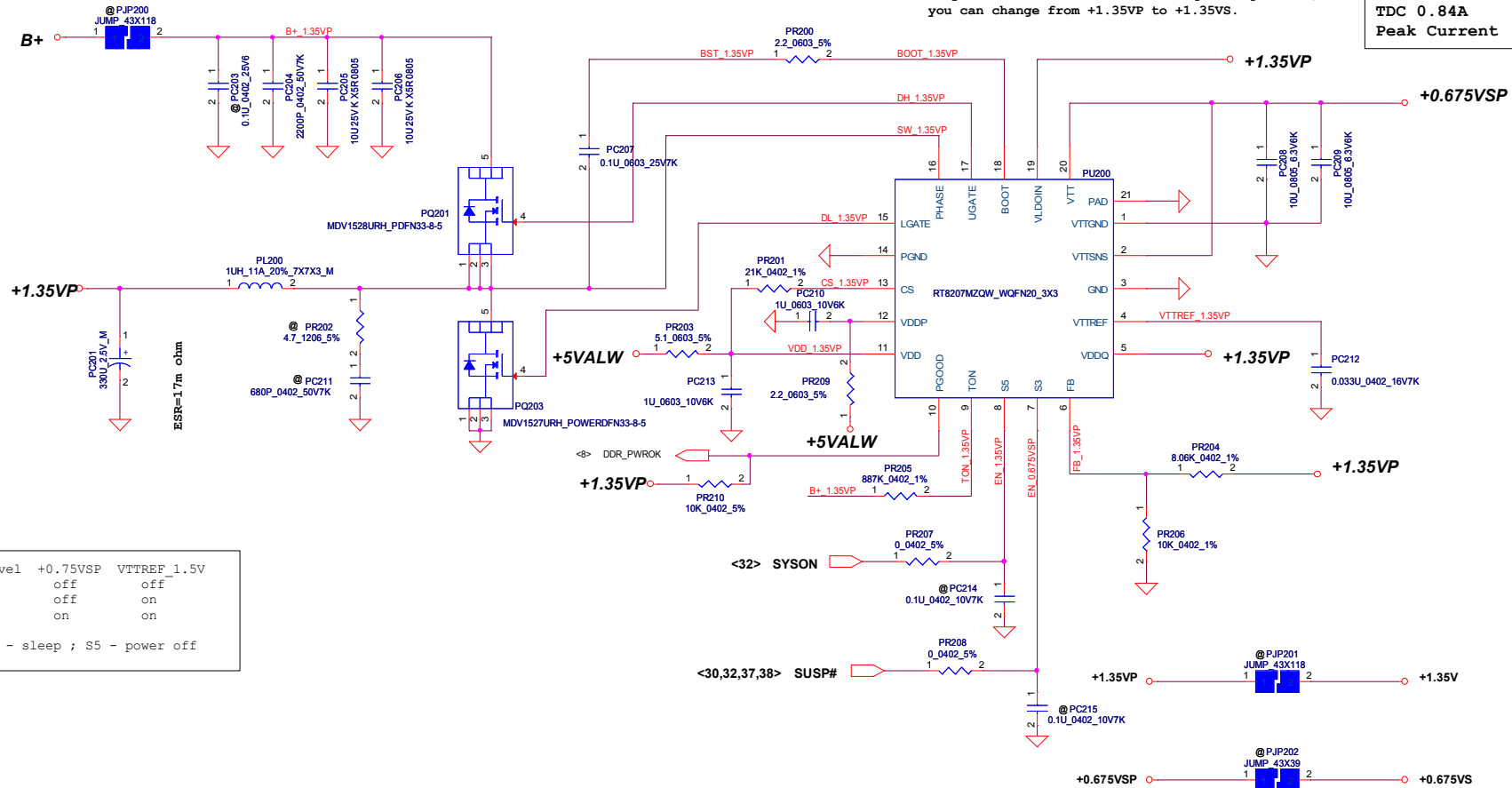
```
1.35VP
TDC 6.87A
Peak Current 9.81A
OCP current 11.77A
```

H/S main Rds(on) :typ:23.2mOhm, max:27.8mOhm
2nd Rds(on) :typ:27mOhm , max:34mOhm

L/S main Rds(on) :typ:19.7mOhm, max:23.7mOhm
2nd Rds(on) :typ:19mOhm , max:23.5mOhm

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.84A
Peak Current 1.2A

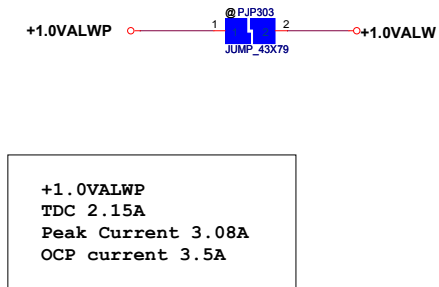
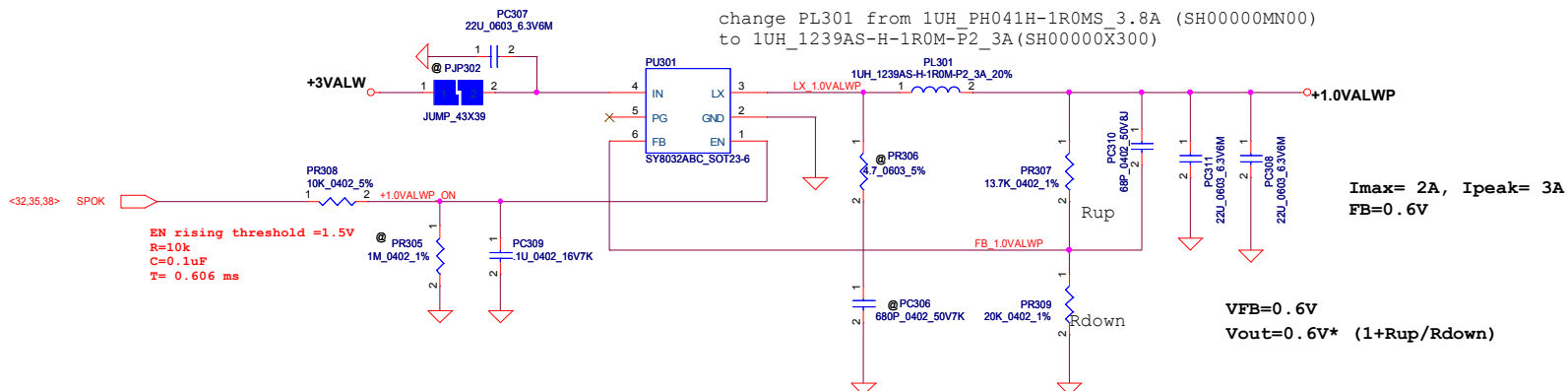
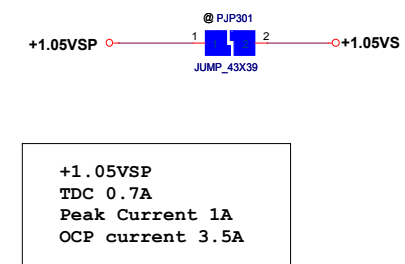
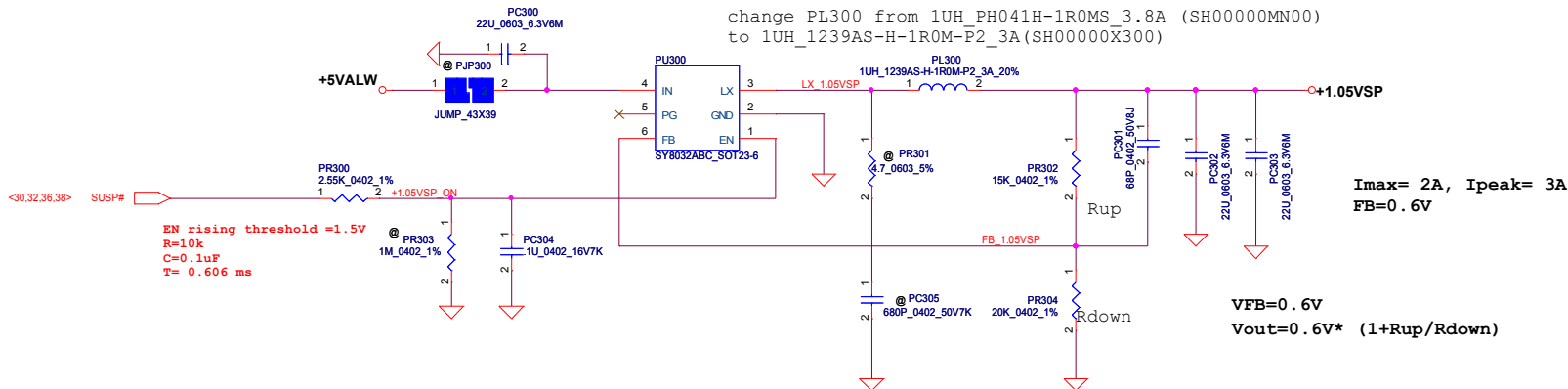


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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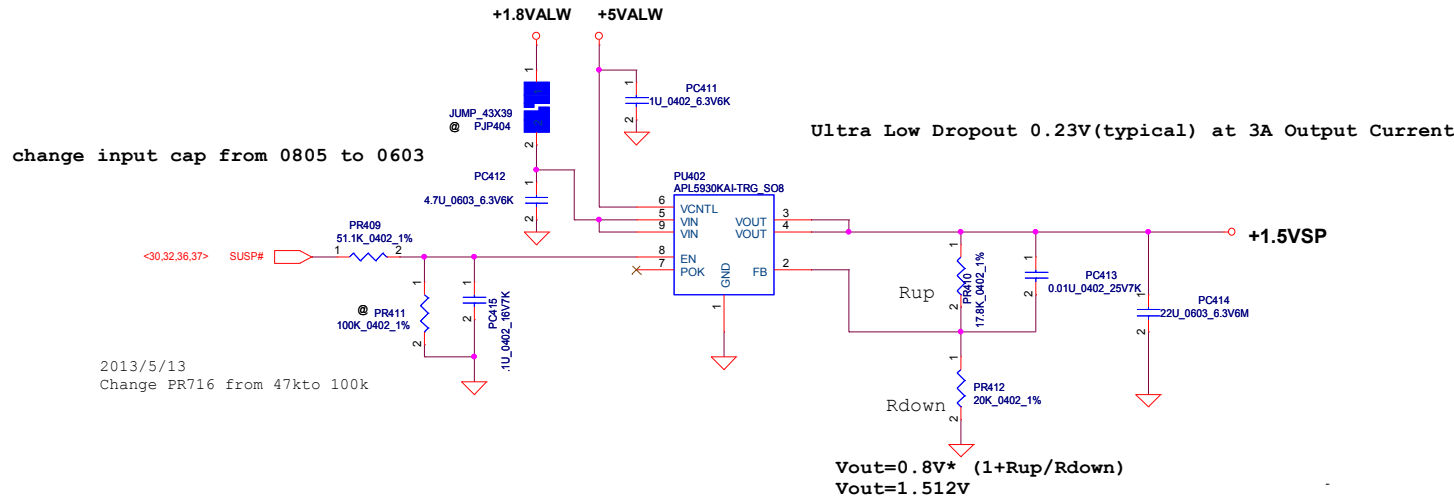
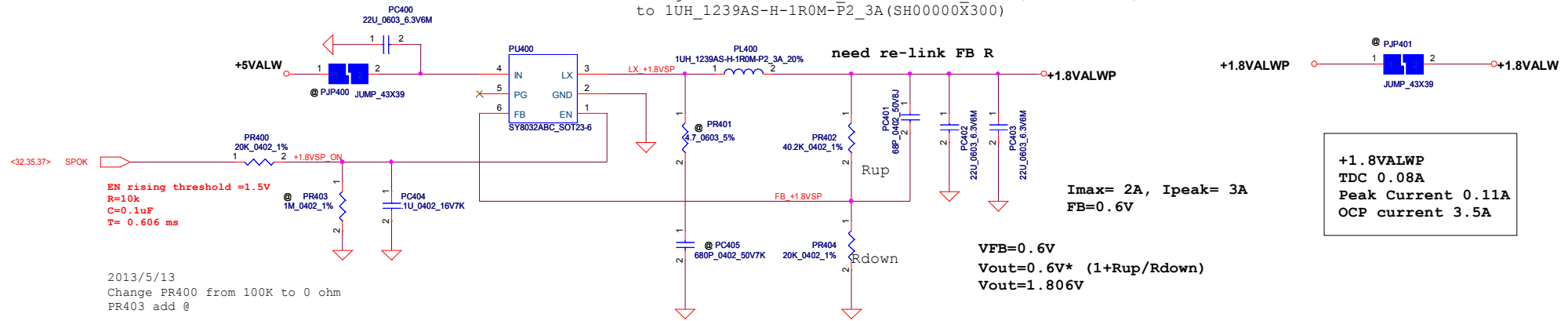
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								P34-PWR-1.05VSP/1.0VALWP			
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						Custom		LA-B481P		2.0	
						Date:		Sheet		37 of 42	

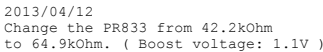
change PL400 from 1UH_PH041H-1R0MS_3.8A (SH00000MN00)
to 1UH_1239AS-H-1R0M-P2_3A(SH00000X300)



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```
2013/04/12
Change the PR808 from @ to 21kOhm.
( Freq: 450kHz )
Change the PR807 from 422 Ohm to 158 Ohm.
( OCP_VNN: 15A )
Change the PC815 from 0.047uF to 0.033uF.
( RC Match )
```



2013/04/12
Change the PR841 from 1.91kOhm to 2.21kOhm.
(Droop_VCC: 5.9mOhm)
Change the PC828 from 470pF to 330pF.
(FB RC to GND)

```
+SOC_VNN
Imax = 9.8A
Ipeak = 14A
Iocp(minimum) = 21A
```

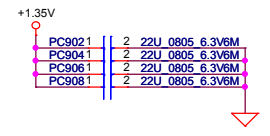
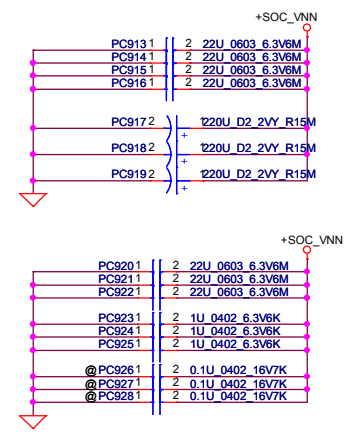
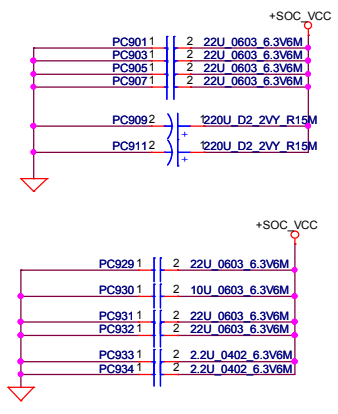
```
+SOC_VCC
Imax = 8.4A
Ipeak = 12A
Iocp(minimum) = 18A
```

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P38-PWR-CPU CORE

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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